An Energy Measurement Method of High-frequency Narrow Laser Pulse based on FPGA

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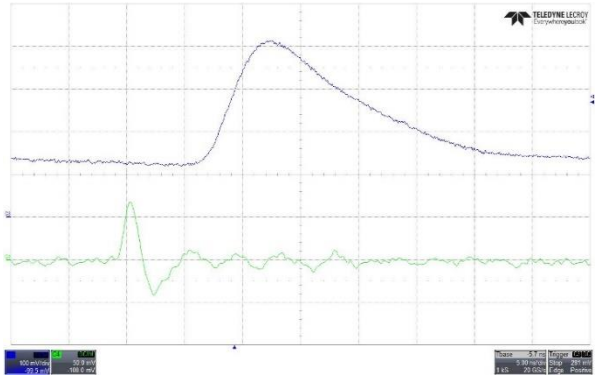

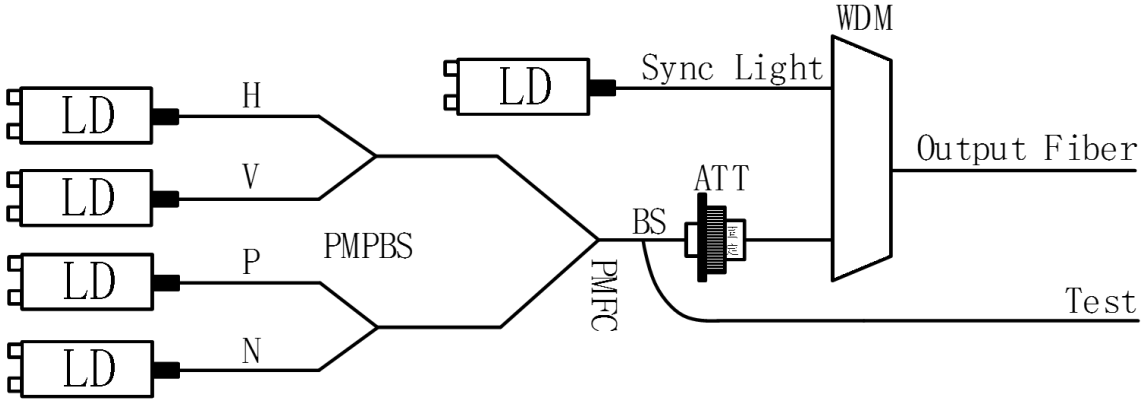

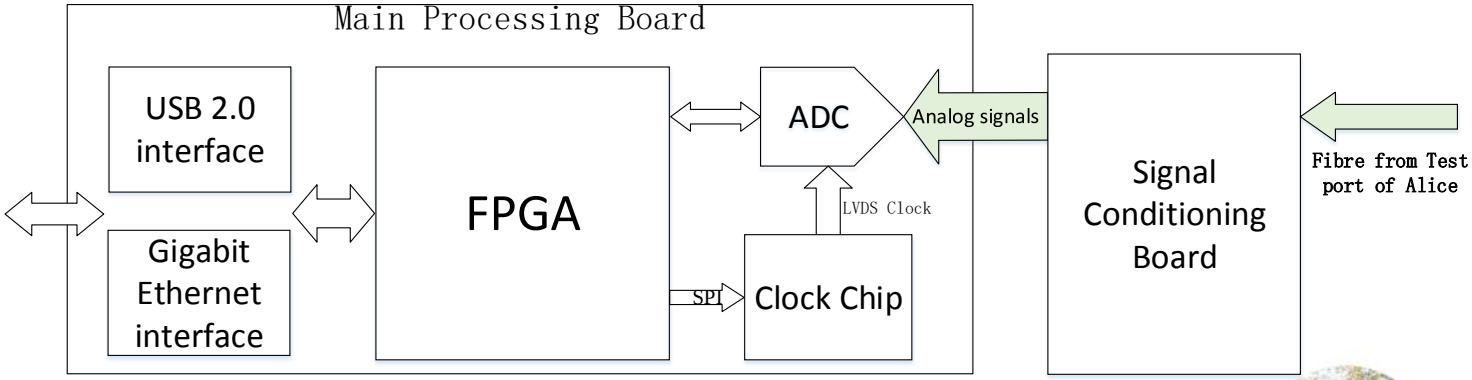

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Introduction

System Design

Data Processing

Test and Result

1.Introduction

With the development of laser technology and high-power lasers, the width of laser pulse is becoming narrower, while the peak power is growing, so that the range of narrow laser application is becoming larger, and now the laser with the pulse width in picosecond level have been applied to the physics, chemistry, biology, quantum communication and other fields for a long time, and playing an increasingly important role. Especially, in the Quantum Key Distribution (QKD) experiment, the pulse width of the laser in transmitter is less than 1ns.

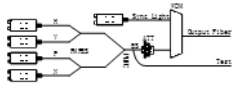

Fig 1. Optics structure of the transmitter

In the QKD system based on the decoy-state-BB84 protocol, a series of laser pulses with random polarization states and intensities are transmitted by the transmitter. There are four polarizations: H, V, P, N and the signal state pulse has an intensity three times of the decoy state pulse while the vacuum state pulse doesn't emit photons. The transmitter also transmits sync-light pulses which have much higher intensities to make sure the information synchronization between the transmitter and the receiver. The sync-light and signal light are coupled into one optical fiber by the WDM technology. In order to debug the system and test the stability of the lasers, the signal light is divided into two paths before coupling and one of the two is connected to the test port of the transmitter as shown in Fig.1. The stability of the lasers and whether the system is working properly can be known by measuring the energy of laser pulses from the test port as shown in Fig. 1.

2.System Architecture Design

The designed system consists of two parts: signal conditioning board and a main processing board with a high speed pipeline ADC, which is shown in Fig.2..

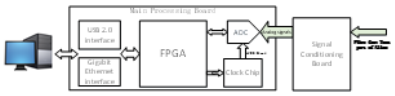

Fig.2 Structure of the energy measurement system

2.1. Signal conditioning

An optical pulse with an about 200ps FWHW from the test port can be converted to a electrical signal with an about 1ns rising edge and 2ns falling edge by a photon diode. The electrical signal is too narrow to be sampled directly so a signal conditioning circuit is developed to amplify and broaden the electrical signal.

The circuit is mainly made of three parts besides a high speed photon diode (PIN), including a non-inverting amplification part, an active filter broadening part and an inverting amplification part as shown in Fig.3.

Fig.3 Signal conditioning circuit

2.2. Main processing board with ADC

The structure of the data processing board including the ADC is shown in Fig.2. The FPGA configures the clock generator via a SPI interface to generate a 200MHz 300MHz LVDS clock to the ADC. As the outputs of the ADC are high speed differential signals, those signal traces should keep the same long length. The length of the two traces inside one differential signal pair should keep 10mils as a margin of error while 50 mils for different pairs. The single-ended Clock trace and data traces of the Gigabit Ethernet Transceiver should be as same long as possible too.

A 10-bit high speed pipeline ADC—AD9211 is selected to sample the analog signal continuously even without synchronous clock. The ADC's sample clock is provided by a high performance clock generator—CDCE62005. Digital data converted by AD9211 are processed inside a high performance FPGA chip—EP3SE100F1152I3 manufactured by Altera Corporation. A Gigabit Ethernet Transceiver—88E1111 is used for transmitting processed data to a computer.

3. Data Processing

The primary functions of the data processing are signal amplitude acquisition and data transmission. They are all implemented inside the FPGA.

3.1. Signal amplitude acquisition

The data come from the ADC are at a 10-bit@300MHz rate that are hardly to be processed directly. So they are deserialized by an on-chip deserializer, then an amplitude acquisition module will receive data from the deserializer and do the associated processing to obtain the amplitude. The deserialization factor is set to 10. So ten parallel data will be outputted with a synchronous clock at 30MHz. Each parallel data has a ten-bit width. The relationship is shown in Fig.5.

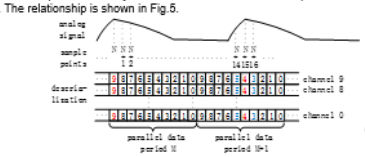

Fig. 5 The relationship of the data before and after deserialized

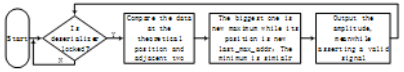

Fig. 6 Flowchart of the signal amplitude acquisition module

There are 15 sample points per analog signal period. The current peak's position will be the position that previous peak's position (last_max_addr) plus 15 ideally. Suppose the last_max_addr is 9 (the highest bit of last parallel data), the current theoretical peak's position will be 4 in the current parallel data as the red numbers shown in Fig.6.

3.2. Data transmission

Data will be reduced to about 200Mbps after data processing and will be uploaded by the Gigabit Ethernet interface based on the media-access-control (MAC) protocol. Altera Corporation offers the Intellectual Property (IP)--The Altera Triple-Speed Ethernet MegaCore Function (TSE) that can supports communication on MAC layer. The TSE supports 10/100/1000-Mbps Ethernet applications and is easy for use.

4.Test

After multiple simulations and experiments, if the resistors and capacitors shown in Fig.3 choose: R1=100Ω、R2=200Ω、R3=200Ω、C1=100pF、C2=5pF, then the broadening will be preferably. Fig.7 shows the comparison before and after conditioning.

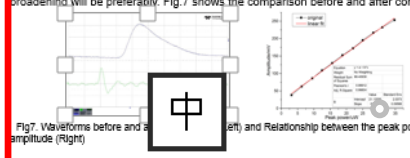

Fig7. Waveforms before and after conditioning (Left) and Relationship between the peak power and the amplitude (Right)

The signal conditioning circuit presents fine linearity within a certain range of peak power. When the peak power is under 35uW, the slope of the line fit curve is about 6.84. The relationship between the peak power of the optical pulse and the amplitude of the electrical signal is shown in Fig.7.

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