



A cosmic ray readout system for qualifications of small-strip Thin Gap Chambers of the ATLAS Muon Spectrometer Phase-I upgrade

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System Development

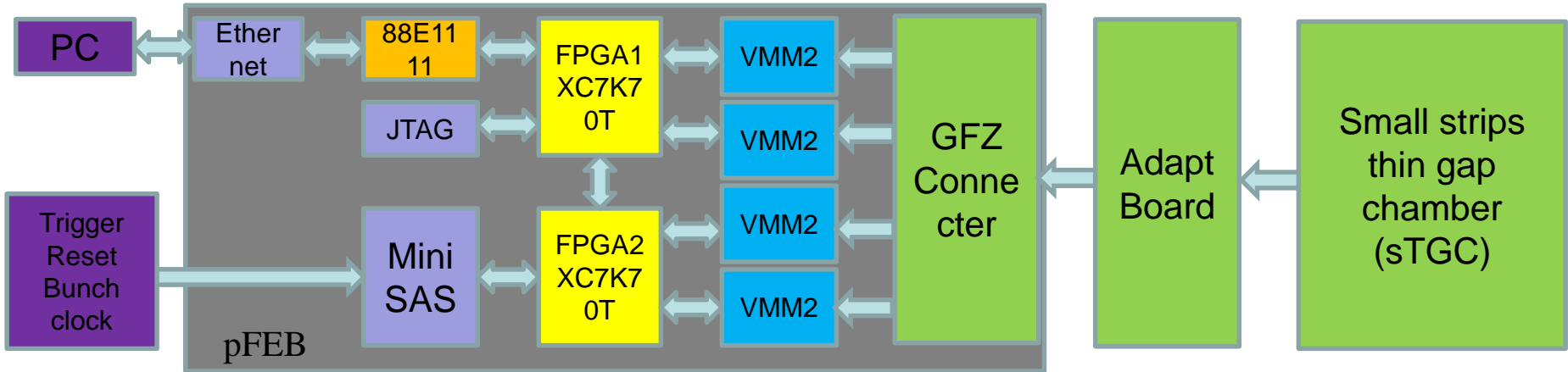


Fig.1 The block diagram of the cosmic ray readout system.

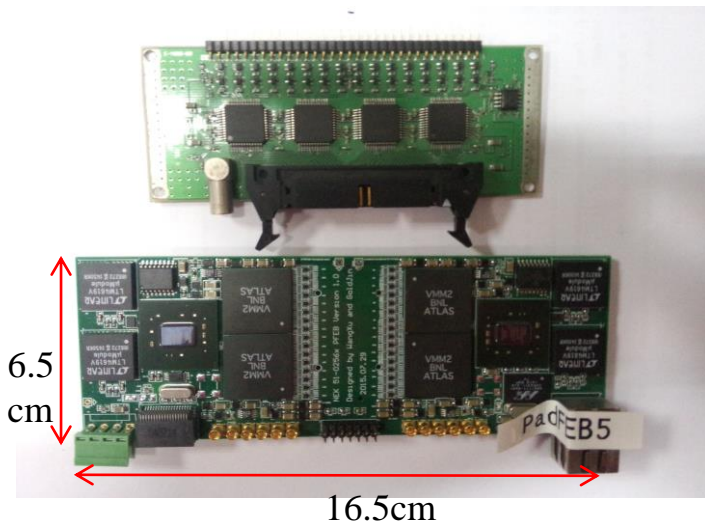


Fig.2 Photo of the pFEB

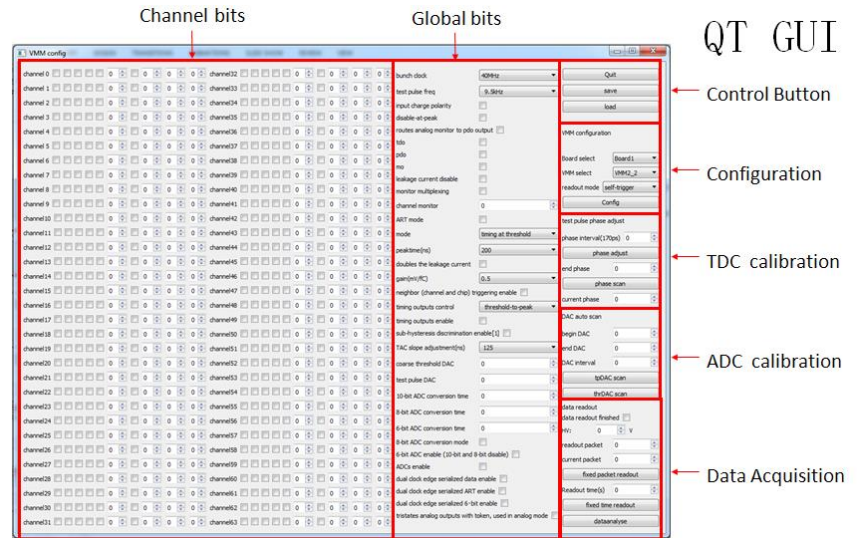


Fig.3 Interface of the host computer software





Experiment Results

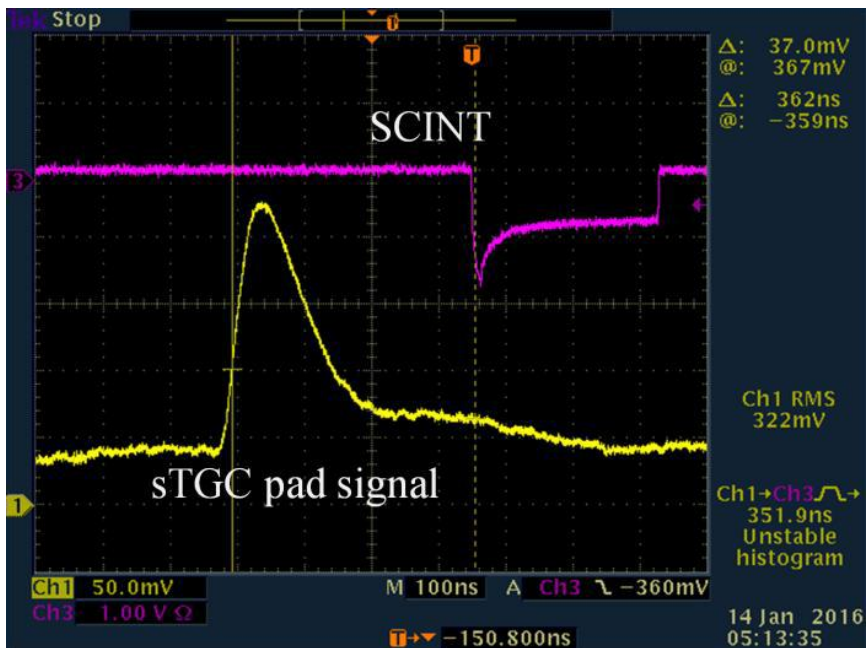


Fig.1 The analog signal of sTGC pads

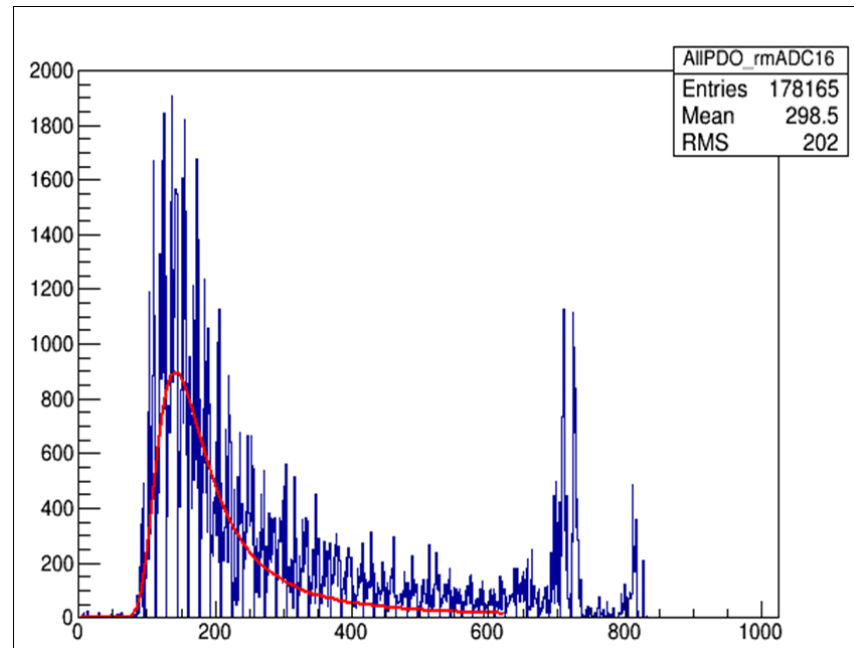



Fig.2 The charge distribution of sTGC pads signals



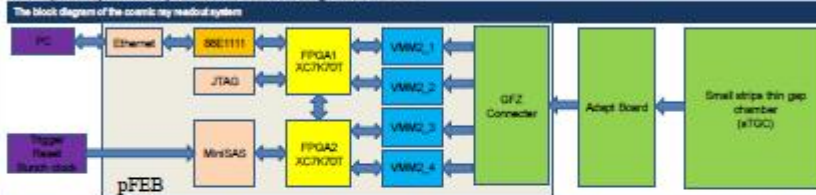
A cosmic ray readout system for qualifications of small-strip Thin Gap Chambers of the ATLAS Muon Spectrometer Phase-I upgrade

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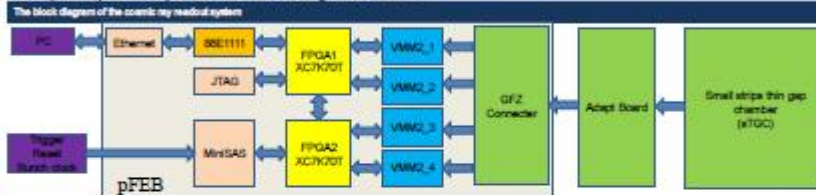
Introduction: The ATLAS experiment at the CERN Large Hadron Collider (LHC) will be upgrading its Muon Spectrometer during LHC phase-I upgrade in around 2019 to benefit from high luminosity and high energy runs at the LHC. The upgrade will replace the innermost station (namely Small (MSM) of the Muon Spectrometer in the forward region with the so-called New Small Wheel (NSW). In order to improve its Level-1 trigger in the high background rate environment. The NSW employs two types of high rate capable gaseous detectors, namely MicroMesh Gaseous Structure (Micromegas) and small-strip Thin Gap Chamber (sTGC), for on-line reconstruction of muon segments with pointing accuracies of 1 mrad. sTGCs, primary trigger detectors, similar to those Thin Gap Chambers instrumented in the present ATLAS Muon Spectrometer but with fine-pitch readout strips, will utilize about 400k readout channels to discriminate bunch crossing in 25 ns and determine hit positions with a precision of about 100 μm per detector layer. Stringent requirements on the timing and spatial measurement precisions, large number of readout channels all impose significant challenges to both the detector construction as well as readout electronics system designs. The readout front-end boards under development for the sTGC detector will carry four 16-channels amplified amplifier and digitization ASICs, four trigger data processing ASICs as well as readout and slow control chips. These boards are expected to carry hundreds of channels of sensitive analog signals as well as high speed serial lines with speeds up to 4.8 Gbps to shift out trigger data off detectors. Large amount of data to be processed on detector and moved out in both trigger and precision readout paths with low latency requirement are of big concern. We will present the development of the first prototype of the front-end board for the sTGC detector, readout scheme and firmware for the mini data acquisition system that has been used to characterize the amplifier and digitization ASIC as well as for integration test with a prototype detector. Results from the front-end board and the prototype detector integration as well as plans to develop a full data rate acquisition system to verify the front-end electronics design will be discussed.

The block diagram of the cosmic ray readout system



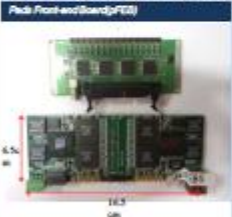
The signals of the sTGC prototype detectors (pads, strips and wires) are gathered by an adapt board and then come through the GFZ connector to the pFEB. The GFZ connector has 1920 pins and 256 channels will be used as signal channels and others will be used as ground connections. The 256 signal channels will be sent into the VMM0 chip, which is an application-specific integrated circuit (ASIC) designed specifically to amplify, shape and digitize the signals from the chamber. Information of amplitude and timing of each hit will be recorded. Xilinx-7 FPGAs are used for the configuration and data readout of VMM0 chips. External trigger, noise and bunch clock will also be sent to FPGA via twisted cables for system synchronization and event pickup. Trigger ID and Bunch clock ID are assigned in FPGA for event grouping with different systems. Ethernet will be used for communication with PC, including monitoring commands and configuration bits and sending data picked from VMM.

Photo of front-end board (pFEB)



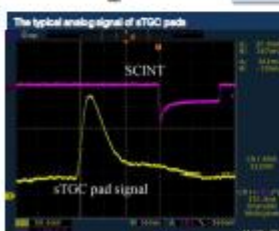
This is a photo of our pFEB (bottom) and the former FED (top). As you can see, the pFEB is designed with a size of 8.5cm*16.5cm in order to be installed on the limited space on the detector, which is about the same size of the former front-end board. However, there are 256 input channels on the pFEB instead of 16 on the former FED. In addition, pFEB can achieve much more functions like analog and digital output, Ethernet communication, data storage and analysis with FPGAs and external trigger.

Graphical User Interface on PC



A graphical user interface (GUI) based on QT is developed for the configuration and data readout. The GUI sends commands and receive data from pFEB through Ethernet. Pcap library is used to get access to Ethernet. The GUI will capture the data and save the data to a binary file. Some simple analysis with the data can be done with the GUI in order to monitor the readout system.

The typical analog signal of sTGC pads



This is a typical analog signal observed with oscilloscope. The signal is triggered by the scintillators. The amplitude and timing information are digitized and sent to FPGA.

The amplitude distribution of a sTGC pad

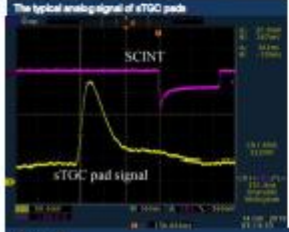


Fig. 3 shows the amplitude distribution of over 17k hits over sTGC prototype pad by cosmic ray which are picked up by external triggers under the high voltage of 2300V. The gain we use is 1 mV/HC. The distribution is reasonable and the readout system can meet the design purpose for a sTGC qualification.

Conclusion

In this paper, a cosmic ray readout system has been built for small-strip Thin Gap Chamber (sTGC) qualification. We designed the pads front-end board and a DAC prototype based on FPGA with Ethernet communication to PC and external trigger acceptance. Test results show that the system is able to measure the noise rate, efficiency, amplitude and timing which are important for a sTGC qualification.

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