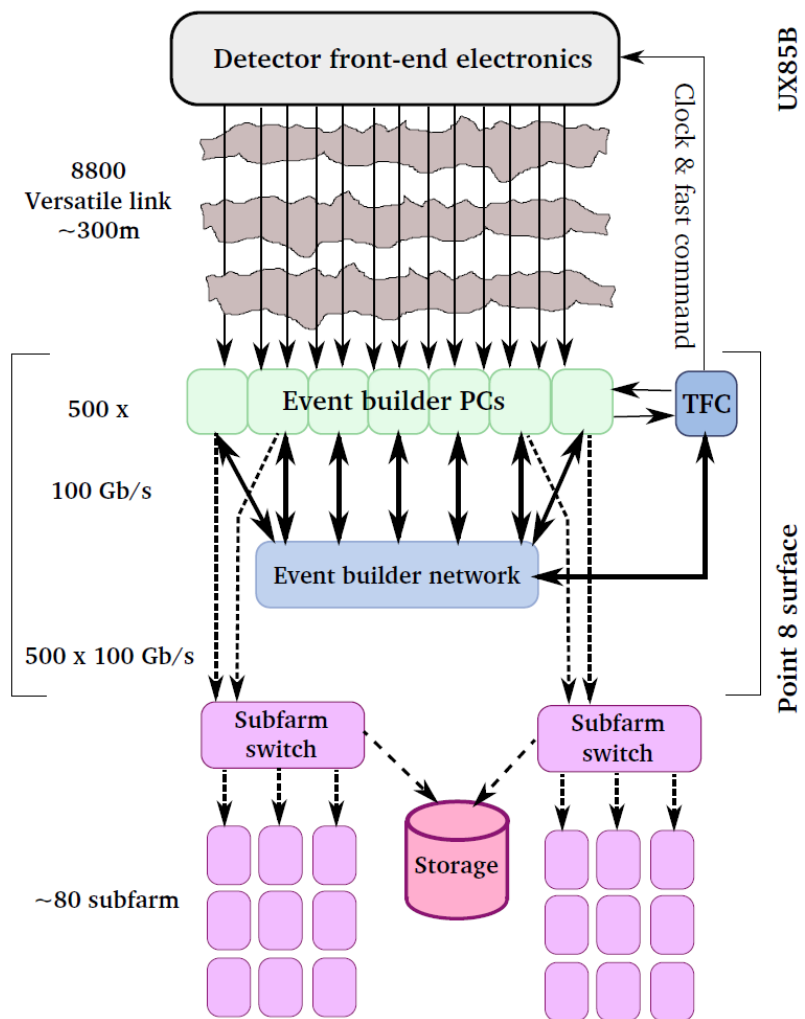
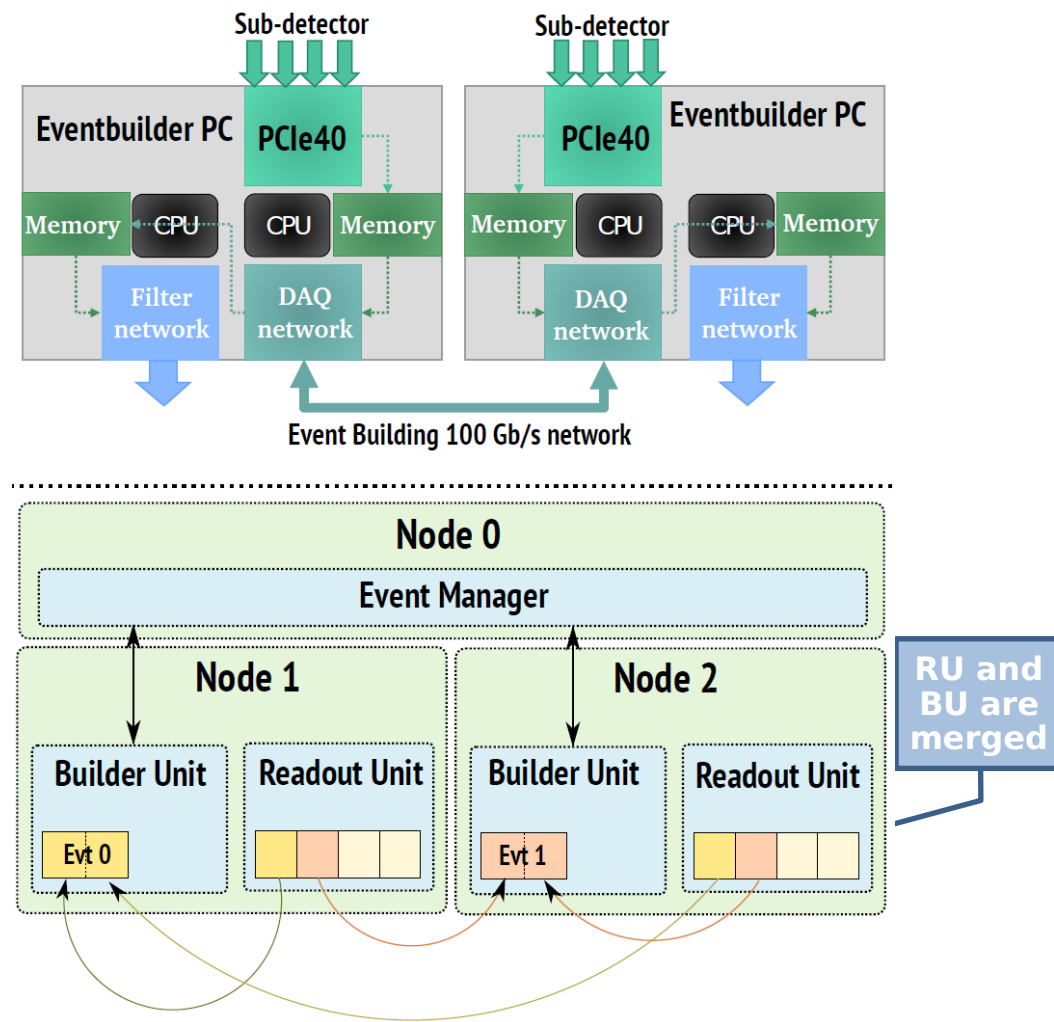


## The architecture of the upgraded LHCb experiment readout-system:



## Event building data flow:






# Evaluation of 100 Gb/s LAN networks for the LHCb DAQ upgrade



Balázs Vőneki and Sébastien Valat




## Poster 229





### Evaluation of 100 Gb/s LAN networks for the LHCb DAQ upgrade

Balázs Vőneki<sup>1</sup>, Sébastien Valat<sup>1</sup>, Jon Machen<sup>2</sup>, Niko Neufeld<sup>1</sup>  
<sup>1</sup> CERN, <sup>2</sup> Intel

*On behalf of the HFC Project*  
 CERN, Geneva, Switzerland  
 June 2016



#### 1 How the LHCb DAQ works today

**Numbers:**

- Collisions happen every 25 nanoseconds
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- Limited to simple algorithms
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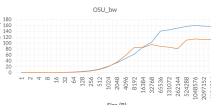
**Numbers:**

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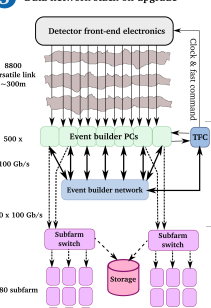


#### 9 Iperf on Intel® Ruby Rapids 100 Gb/s

2 parallel iperf3 instances, 50 threads/port1, window size varies from 32 KB to 256 KB



#### 3 Data network stack on upgrade



#### 6 Our benchmark & status

We implemented the DAQPIPE[1] benchmark to evaluate the available solutions for the DAQ event building part.

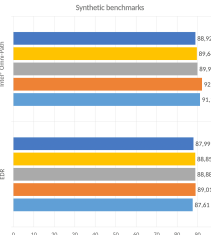
Current tests have been done on 100 Gb/s networks up to 16 nodes and showed access to bandwidth of 85 Gb/s per node.

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Experimentation with some synthetic benchmarks (one synchronisation, just sending packets) with various communication topology, scheduling and mix of message sizes to evaluate potential effects on the network. With DAQPIPE we are close to the GatherCmndMeta case.



#### 4 100 Gb/s network technologies

**EDR InfiniBand & Intel® Omni-Path**

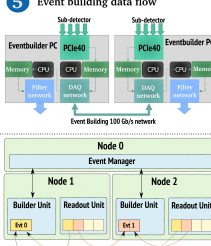
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- Speeds for 4x links : 100 Gb/s
- Provides RDMA for low CPU overhead
- Optimized for HPC deployments



**100 Gb/s Ethernet**

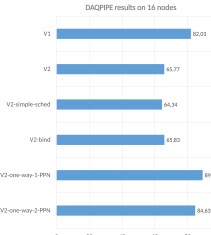
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- Interest for event building and filter farm

#### 5 Event building data flow



#### 11 DAQPIPE benchmark on InfiniBand

Evolution with the DAQPIPE benchmark using different versions and running modes on 16 InfiniBand EDR nodes. Best result are obtained by using only one task (sending or receiving) per process, not mixing the two, cf. one-way and v1.





# Evaluation of 100 Gb/s LAN networks for the LHCb DAQ upgrade



Balázs Vőneki and Sébastien Valat



## Poster 229

Introduction →

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Balázs Vőneki and Sébastien Valat



## Poster 229

Introduction



Architecture



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**3 Data network stack on upgrade**  
 Diagram showing the data flow from Detector front-end electronics (8800 Versatile Link ~300m) through Event builder PCs (500 x 100 Gb/s) to Subfarm switches (~80 subfarm) and Storage.

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 Diagram showing Eventbuilder PC (PCle40) and Sub-detector (PCle40) connected to Event Building 100 Gb/s network. Node 0 (Event Manager) connects to Node 1 (Builder Unit) and Node 2 (Readout Unit).

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 Graph showing network communication monitoring over time.

**8 OSU benchmark on Intel® Omni-Path**  
 Graph showing OSU benchmark results for different network configurations.

**9 Iperf on Intel® Ruby Rapids 100 Gb/s**  
 Graph showing Iperf results for different window sizes (32 KB, 64 KB, 128 KB, 256 KB).

**10 Synthetic benchmark on HPC networks**  
 Graph showing synthetic benchmark results for various communication topologies and message sizes.

**11 DAQPIPE benchmark on InfiniBand**  
 Graph showing DAQPIPE benchmark results on 16 nodes for various versions (V1, V2) and configurations (simple-sched, 1-1FN, 2-1FN).

Introduction →

← Architecture

Various benchmark results →