Data Chain Reconstructing Technology for the front-end electronics of the BESIII muon identification system

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Introduction and design

The readout electronics for the BESIII muon identification system is comprised of 40 data chains. The structure of a data chain and of the data stream is illustrated in Fig. 1. Each data chain consists of 16 FECs, which are connected in daisy chain mode via cascade cables.

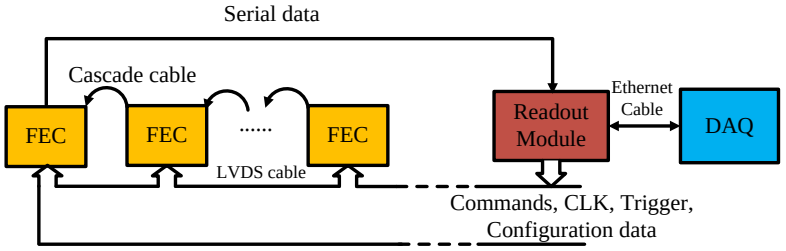

Fig. 1 The structure of a data chain and of the data stream

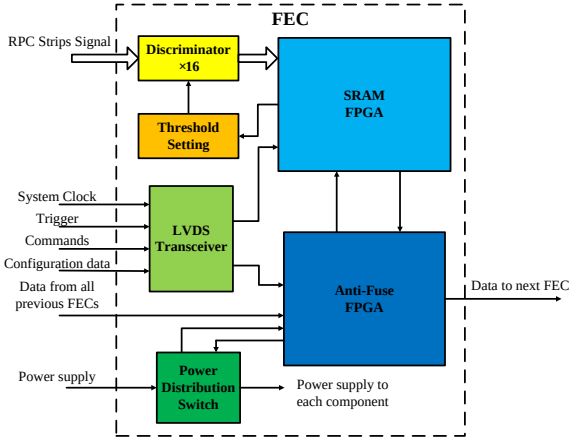

Fig. 2 Implementation sketch of FEC

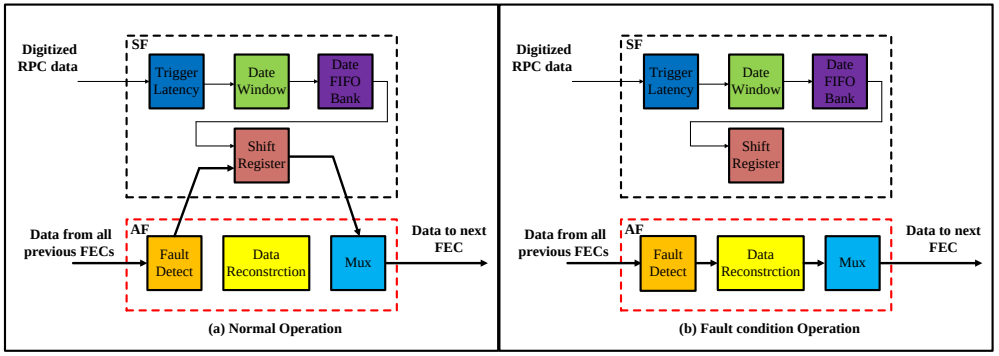

Fig. 3 The operational diagram of the data processing logic

However, this technique has an obvious limitation in that the failure of a single component will disable the entire data chain.

In order to automatically disconnect malfunctioning front-end cards and reorganize the data transmission channel to minimize the loss of data. The original FEC design is modified to achieve a data chain reconstruction function. The new designed FEC uses a SDRAM based on FPGA (SF) and an anti-fuse based FPGA (AF), which carry out all the logical functions required for processing digital data. Fig. 2 shows an implementation sketch of the FEC. Fig. 3 displays the general operational diagram of the data processing logic.

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1.Introduction

To reduce the cost and minimize the occupying volume of the transmission cables in the spectrometer, some middle and low energy particle physics experiment employ serial daisy-chain techniques, which organize the front-end cards (FECs) in a daisy-chain topology, and data is transferred in a serial mode from FECs to the rear-end electronics[1,2,3]. However, this technique has an obvious limitation in that the failure of a single component will disable the entire data chain. As the only solution, a data chain reconstruction technology is proposed based on the front-end electronics of the Beijing Spectrometer (BESIII) muon identification system. This technology can automatically disconnect malfunctioning front-end cards and reorganize the data transmission channel to minimize the loss of data. In this paper, we report our work on the design of data chain reconstruction, focusing on the realization of data reconstruction using highly reliable anti-fuse field programmable gate arrays (FPGAs), on the prevention of short circuits, and on fault tolerance improvement. A prototype of the reconstructing data chain designed for the front-end electronics of the BESIII muon identification system has fulfilled the requirements of a laboratory environment and is able to now be applied in an actual experiment.

2.Data Chain Structure

The readout electronics for the BESIII muon identification system is comprised of 40 data chains[4]. The structure of a data chain and of the data stream is illustrated in Fig. 1. Each data chain consists of 16 FECs, which are connected in daisy chain mode via cascade cables. The tasks of the FECs are to transform the information from Resistive Plate Chamber (RPC) strips into digital data, handle the data of the event after the trigger signal, store the data into the sub-event buffers with the appropriate header and wait for the call by the Data Acquisition (DAQ) system. The output of each FEC is a 16-bit serial stream and is connected to the next FEC in daisy chain mode. At the end of the data chain (far left in the figure), the data from all 16 FECs' are converted into the low voltage differential signaling (LVDS) format and transmitted to the readout module through a 30m long shielded twisted pair cable by the final FEC. Control commands, clocks, triggers and configuration data are also transmitted via this cable.

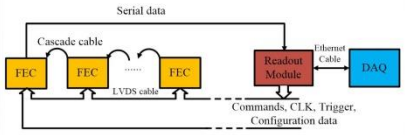

Fig. 1 The structure of a data chain and of the data stream

3.FEC Design

The original FEC design is modified to achieve a data chain reconstruction function. The new designed FEC uses a SDRAM based on FPGA (SF) and an anti-fuse based FPGA (AF), which carry out all the logical functions required for processing digital data. Fig. 2 shows an implementation sketch of the FEC. Besides the FPGAs, four other types of components are adopted for different tasks[5]. The discriminator component, whose threshold level is set by the threshold setting circuit, performs signal detection. The power-distribution switch and the LVDS transceiver components are responsible for the power supply monitoring and control of each component and the electric level conversion, respectively.

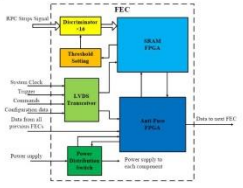

Fig. 1 The structure of a data chain and of the data stream

3.1 FPGA logics

The Actel AM series anti-fuse FPGA was chosen as the AF, which provides several benefits such as high reliability and live at power-up capability, with no secondary support components required, along with increased tolerance to certain radiation effects. Due to its very high reliability and stability, the AF is very difficult to damage. In this premise, Fig. 3 displays the general operational diagram of the data processing logic.

Under the normal operation conditions, as shown in Fig.3 (a), the digitized RPC data coming from 16 channels are stored in the FIFOs of SF waiting for the trigger signal. The output of the shift registers become a 16-bit serial stream and connected to the data from all previous FECs when the trigger signal occurs. The AF just supplies a data path for the serial chain data.

When a fault occurs in a certain FEC, the power supply of this FEC is cut off except for the AF. In this case, as shown in Fig.3 (b), the fault detection module of AF is commanded to output data to the data reconstruction module, in which data losses of the RPC information is compensated by bits "0" and fault flag in order to keep consistent with the data format of the normal operation conditions.

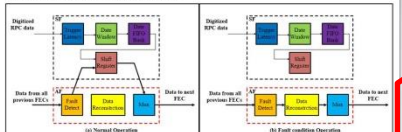

Fig. 3 The operational diagram of the data processing logic

3.2 Power control and Redundancy design

As for the data chains installed inside a detector, the environment around a FEC can be so adverse that any fault condition is possible, even short circuits. Once a short circuit is encountered in a particular FEC, the normal operation of the entire data chain may be permanently disrupted.

To solve this problem we employ a current-limit power-distribution switch in each FEC, which can limit the output current to a safe level and automatically cut off the power supply with the assertion of a fault signal in response to a short circuit.

Finally, to improve the fault tolerance, some redundancy hardware is designed, including a redundancy power supply for the AF and the LVDS transmitter chips.

5.Test Results

- ✓ **Normal work mode test**
  - ➢ The normal work mode test employed a trigger rate of 1 k Hz corresponding to the threshold of 40 mV, and no data lost or error in a 24-hour test period.
- ✓ **Abnormal work mode test**
  - ➢ In the abnormal work mode test, the power supply for SF as well as comparators and the DAC were cut off to simulate a condition of damage. The results indicated that the data chain achieved the data reconstruction function as expected, as shown by the following.
    - a) The normal work mode FECs performed well with no data lost or errors incurred.
    - b) The data format did not change compared with normal work mode.
    - c) The data for breakdown FECs were "0", which do not influence the detector hit count histogram.
- ✓ **Short circuit test**
  - ➢ In this test, a short circuit was artificially introduced into a normally functioning data chain to determine whether the power-distribution switches were able to cut-off the power in a timely fashion and provide an assertion of a fault signal to the anti-fuse FPGA. The result indicated that the power was cut off within 10 ms after the short circuit occurred and an alarm signal was sent to the anti-fuse FPGA to notice which to performance data reconstruction function.

6.Conclusions

In this paper, a latest data chain reconstruction technology was presented. The technology, which is proposed for the first time in the world, provides automatic disconnection of malfunctioning boards and data reconstruction functions to minimize data loss. This method is proposed and developed based on the front-end electronics of the BESIII muon identification system. Test results indicate that the design is feasible and reliable and it will be applied in the future to an actual BESIII experiment.

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