“NaNet: FPGA-based Network Interface Cards Implementing Real-time Data Transport for HEP Experiments”

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on behalf of NaNet collaborations

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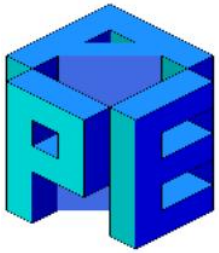
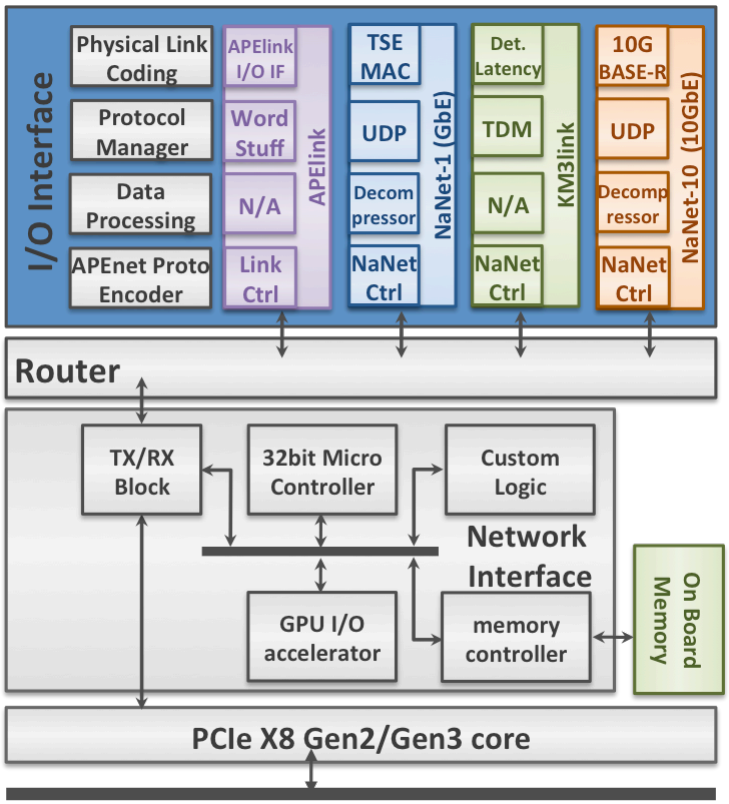
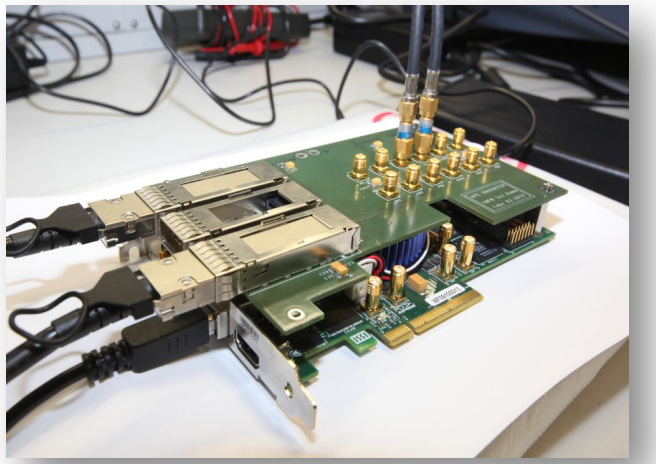


NaNet

NaNet project goal is the design and the implementation of a family of FPGA-based PCIe Network Interface Cards implementing low-latency, real-time data transport between its network channels and the the CPU/GPU memories.

A reconfigurable processing module is also available to implement application-specific processing on inbound/outbound data streams with highly reproducible latency.





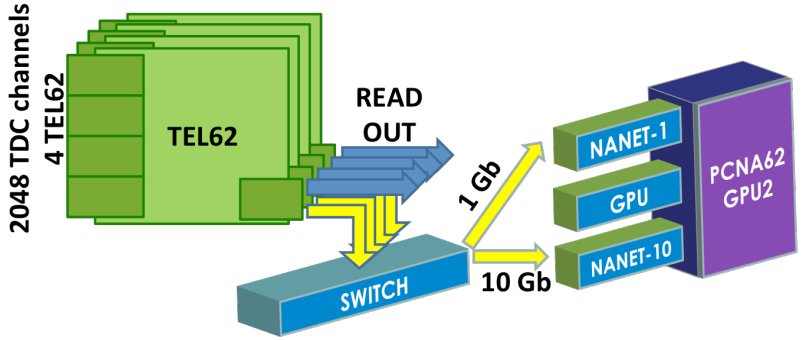
NaNet-1 is based on Altera Stratix IV dev board

As of now NaNet design has been specialized in:

1. NaNet-1 (single 1GbE port)
2. NaNet-10 (four 10GbE ports)

employed in the GPU-based real-time trigger of the CERN NA62 experiment

SEE ALSO THE TALK ON FRIDAY 8:30 A.M.



3. NaNet3 (four 2.5 Gbit optical channels)

adopted in the data acquisition system of the KM3NeT-Italia underwater neutrino telescope.