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High Speed Ethernet Application for the Trigger Electronics of the New Small Wheel

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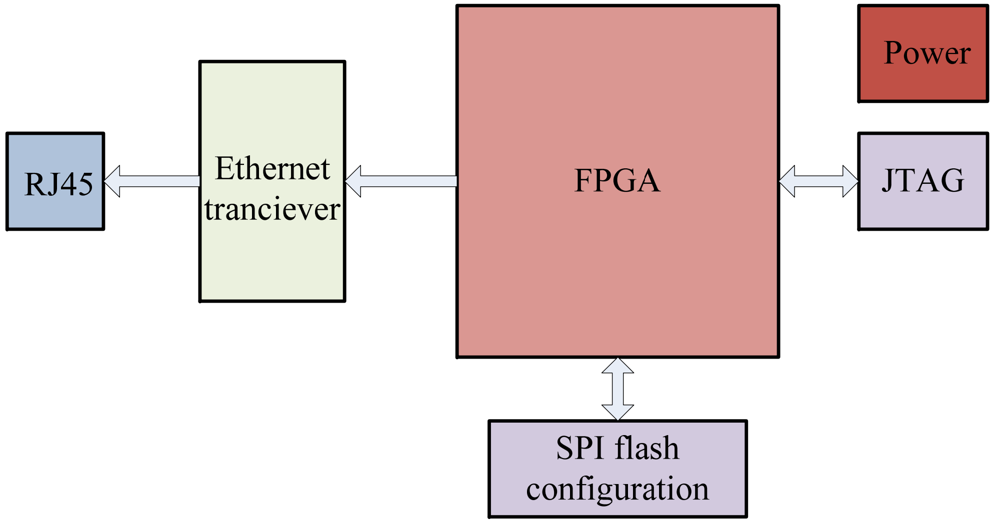
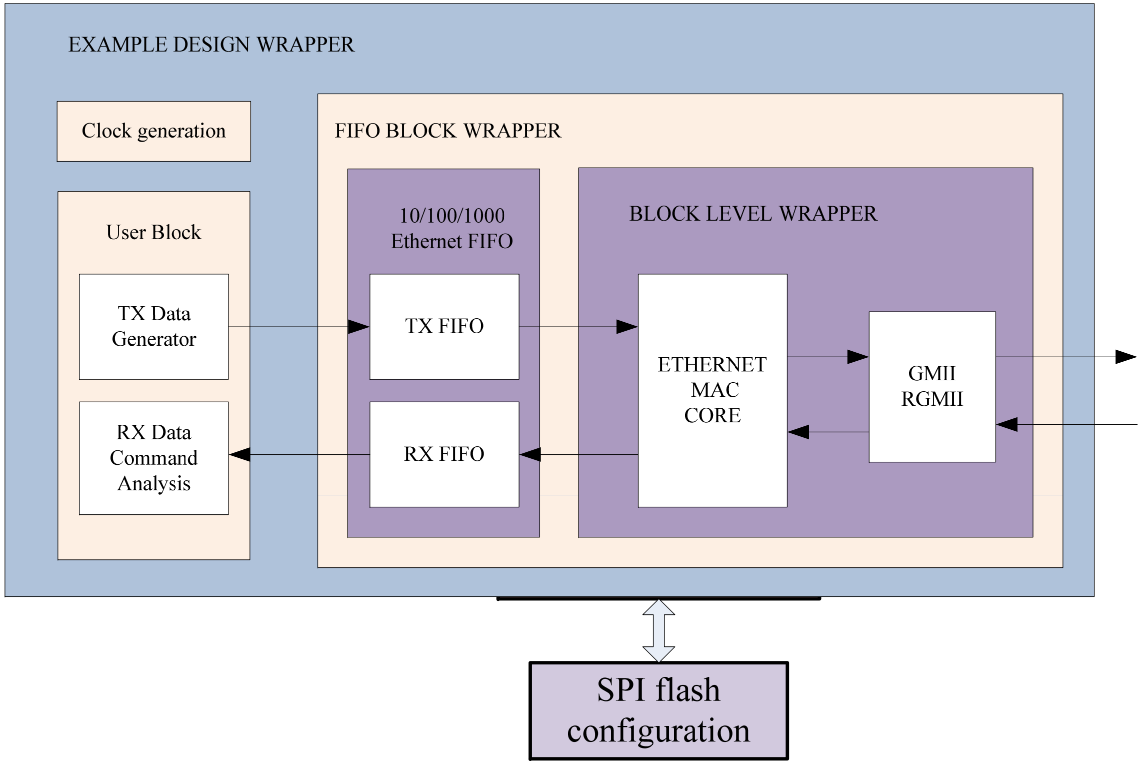
- The GEM (gigabit Ethernet module) provides a test platform for the Ethernet.
- The core of the GEM is based on a Kintex-7 FPGA. The Ethernet transceiver with the 1000BASE-T standard is operated at the physical layer.

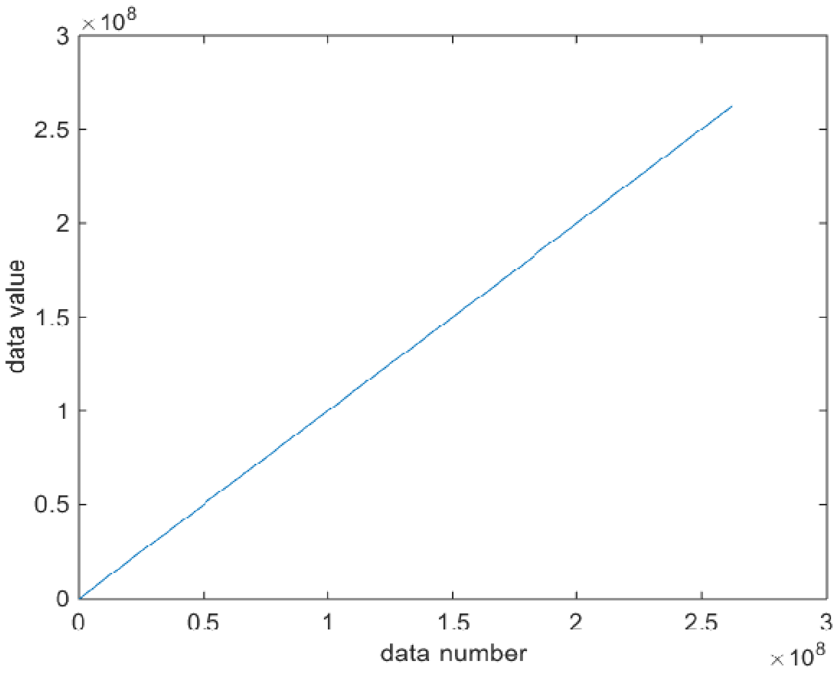


FPGA Ethernet

- The Ethernet MAC core is embedded in the FPGA for implementation of Ethernet data link layer.
- The design includes a basic glue logic brings up the external PHY and MAC to allow basic frame transfer or receive.

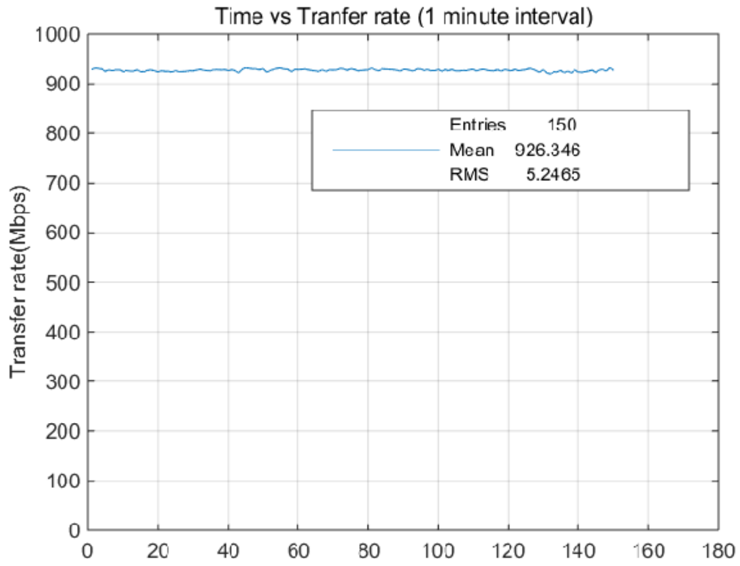


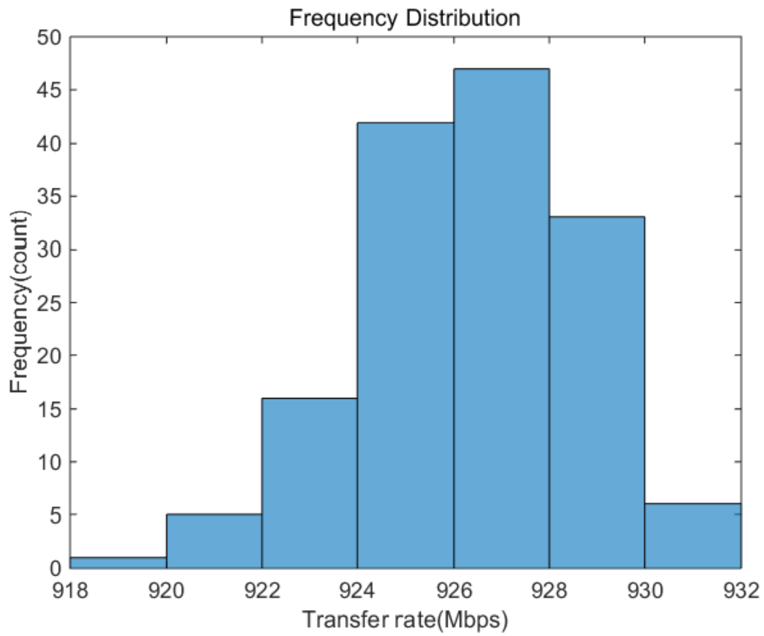
GEM Test



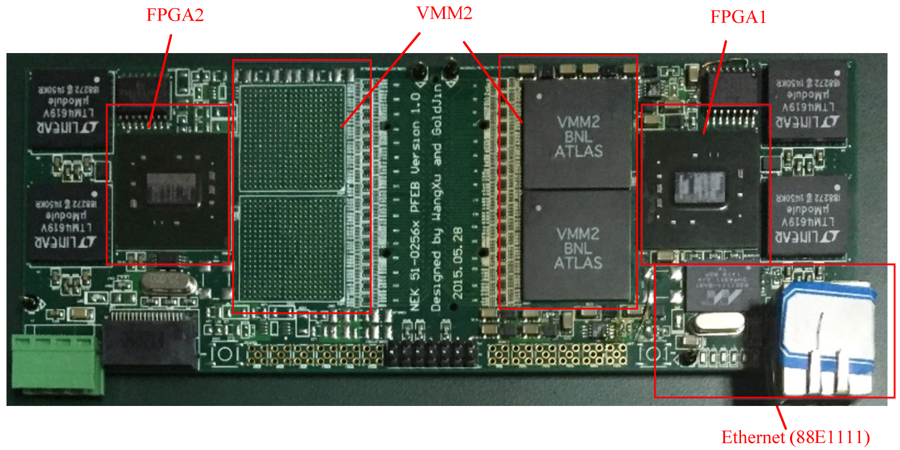
■Linear data correctness test.

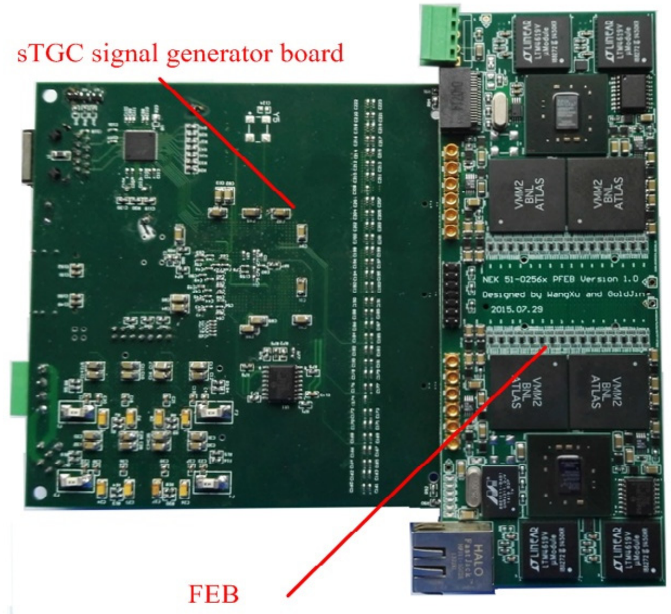
■Transfer speed and stability test. Measure the transfer rate for 150 minutes, sample interval is 1 minute.

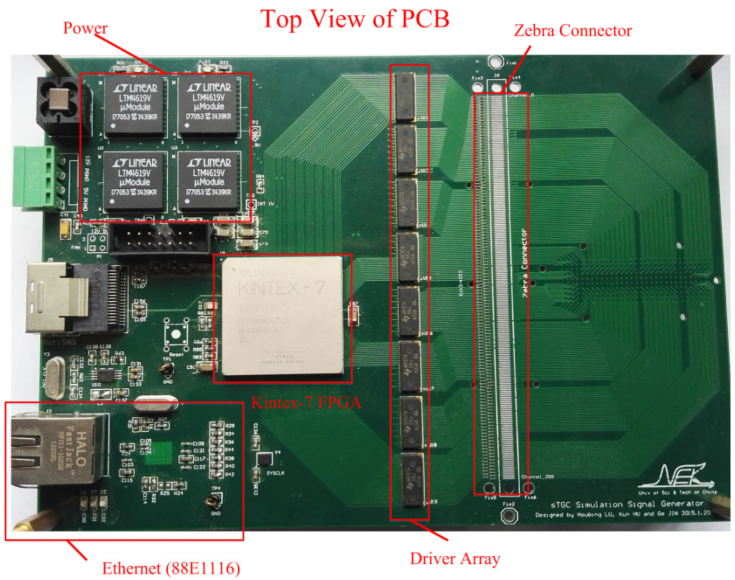




GEM Application







■The GEM prototype has been applied in pFEB (pad frond end board) and SG (signal generator). The Ethernet interface is response for the communication between pFEB and PC or SG and PC.

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Poster

Introduction

GEM Test

GEM Application

GEM Implementation

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1. Introduction

The ATLAS detector will be upgraded in 2018. The main focus of the Phase-I ATLAS upgrade is on the Level-1 trigger, replacing the present muon small wheels (SW) with the "new small wheel(NSW)", which consists of small thin gap chamber(sTGC) and micromegas (MM). A versatile application-specific integrated circuit(ASIC), the VMM chip, have been developed to read out the signals of the sTGC and MM. The VMM have 64 channels. In order to test the performance of the VMM, a large data transfer rate is needed. Meanwhile, it is required to implement the multi-board interconnection. It is proposed to apply the high-speed Ethernet-based network. In this paper, we will introduce a high-speed test platform, the gigabit Ethernet module (GEM). The WinPcap[5] (windows packet capture) technique is used to achieve the communication between the hardware and the computer. The performance of the gigabit Ethernet, including number of lost packets, reliability, and transfer rate, is described below. Subsequently, we apply the high speed Ethernet to pFEB (pad front-end board) and SG (signal generator). The results are presented in detail.

2. GEM IMPLEMENTATION

The GEM provides a test platform for the Ethernet. In the following we describe the architecture of the GEM, this new platform is fully programmable and delivers Gigabit wire-speed performance.

The schematic block diagram of the GEM is illustrated in Fig. 1. The core of the GEM is based on a Kintex-7 FPGA, which is configured by a serial peripheral interface flash. In order to simplify the hardware design, the Ethernet MAC core is embedded in the FPGA for implementation of Ethernet data link layer. The functionality of the MAC is well defined and fixed for Ethernet protocol. Fig. 2 shows TEMAC functional block diagram. In order to have an Ethernet connection, physical layer uses PHY device, and connect PHY device to the FPGA. The Ethernet transceiver with the 1000BASE-T standard is operated at the physical layer. The Alaska 88E1111 Gigabit Ethernet Transceiver is a physical layer device used this containing a single Gigabit Ethernet transceiver and supports the GMII, and the Alaska 88E1116R Gigabit Ethernet Transceiver is a physical layer device used this containing a single Gigabit Ethernet transceiver and supports the RGMII (Reduced pin count GMII), they can direct connection to the Gigabit MAC core block. The RJ45 port implements the connection between the hardware and the computer.

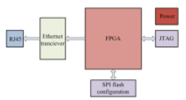

Fig.1 The schematic block diagram of the GEM.

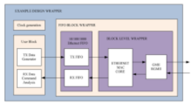

Fig.2 TEMAC functional block diagram.

Applications for network analysis rely on an appropriate set of primitives to capture packets, monitor the network and more. The communication between the servers and the clients is done using the MAC protocol now, Windows capabilities are not satisfying for it is not a standard TCP/IP communication protocol where all computer adopt. so we use WinPcap technology to capture Ethernet packets. WinPcap is the industry-standard tool for link layer network access in Windows environments. WinPcap consists of a driver, which provides low-level network access to capture and transmit network packets directly and bypass the complexity of TCP/IP protocol stack. WinPcap architecture consists of three parts as is shown in Fig. 3.

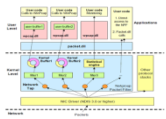

Fig.3 Structure of WinPcap.

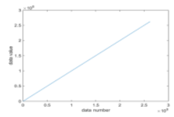

Fig.4 Linear data correctness test.

The basic structure of WinPcap retains some most important modules: a filtering machine, two buffers (kernel and user) and a couple of libraries at user level. WinPcap includes an optimized kernel mode driver, called Netgroup Packet Filter (NPF), which directly interact with the network card drivers to get on the network transmission of the original data packet. Its function is to filter data packets and transmit the data packet to user-level perfectly. Packet.dll, offering a system-independent API, provide a common interface to the packet driver among the Win32 platforms. Pactet.dll can perform low-level operations such as obtaining the name of adapter, dynamic loading driver and some system-specific information of the machine and hardware. WPcap.dll, is Operation System-independent, contains some high-level functions such as filter generation, user-level buffering, statistics and packet injection, which one can easily use.

3. GEM Test

To demonstrate the potential of the GEM, some important attributes of GEM are tested, we implemented the following four test cases:

Correctness test: we monitored the incoming and outgoing signals of the GEM to verify correctness of the hardware interface on the FPGA. In addition, we transfer data from the GEM to a client PC using linear values. the GEM sent 1 Giga bytes to PC every time, the client received data and displayed a linear growth, the test result is shown in Fig. 4, there are no errors in the transmission.

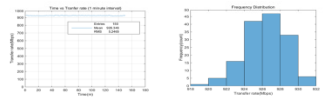

Fig.5 Transfer speed and stability test.

Performance test: We also estimated the transfer speed and stability, for this experiment, the GEM was programmed to transmit user data with 1,280 bytes at a user-define frame, as specified in the IEEE STD 802.3 2002 specification. We controlled the generated rate of these data using a counter in FPGA. The received rate increased linearly when we increased the generated rate. Our tests show a transmission rate higher than 900 Mbps and a success rate is 100%, The test result is shown in Fig. 5. Long term stability of the GEM is also tested, It runs two and an half hours. Also, the packet loss is tested in real time by embedding a sequence number into each packet sent to the computer. The test result is shown in Fig. 5. BER test: We also performed bit error ratio (BER) measurements on the link implemented with our GEM. More than 10^{12} bits have been transferred continuous and no errors have been observed, corresponding to a 10^{-12} BER.

4.GEM Application

The GEM has been applied in a dedicated test situation and has been proven to be robust and to meet performance requirements. We present the projects currently using it in pFEB and SG. A pFEB design based on a ASIC has been developed to read-out pads signals from sTGC dectectors. The second prototype version of this ASIC is called VMM2 chip, which provides the peak amplitude and time with respect to the bunch crossing clock or other trigger signal, in a data driven mode. A VMM2 has 64 channels input, there are four VMM2 chips on each pFEB for sampling 256 channel signal of the sTGC detector. The board can provide Ethernet communication interface and Mini-SAS interface. The architecture of pFEB is illustrated in Fig. 6. The SG concept is based on the test requirements of pFEB or strip FEB (sFEB) which are developing for the future upgrade of the ATLAS NSW Muon detector. It is mainly used to emulate the output of sTGC detector for testing and verifying the FEB electronics and data acquisition system conveniently, checking the performance of FEB. It has been designed into 256 channels and every channel can output a signal for simulating the particles hits the sTGC detector per 25ns. In the process of research and development of FEB, it can test their functions and performances quickly. The SG has been developed as shown in Fig. 7. It can provide 6 modes for test application of pFEB and sFEB.

Fig.6 The photograph of pFEB.

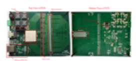

Fig.7 The photograph of SG.

5.Conclusions

The GEM prototype has been developed. The GEM processes the data with Xilinx FPGA and transfers data to a computer via Ethernet with MAC protocol, which is a technology to realize direct access and transfer of the data in the FIFO of FPGA from the PC. The test show that it can achieve a high speed data transfer and long term stability. Two application based on the GEM have been developed, for the test of the pFEB and SG, the GEM can work properly and give excellent results.

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