Readout System with 2-Channel 8-Bit 1GHz FADC Based on RAIN1000Z1 ZYNQ Module for Crystal Detector

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***Abstract*–RAIN1000Z1 is a high performance readout module we developed last two years. It is based on the ZYNQ architecture SOC chip from Xilinx and ZYNQ is the new architecture of FPGA with dual high performance ARM Cortex-A9 processors and high capacity programmable logic. We developed a series of readout system with the RAIN1000Z1 module based on ZYNQ architecture. For the crystal scintillator detectors, such as BC-501A liquid scintillator in a Teflon vessel we used for neutron background measurement in CJPL (China JinPing under-ground Lab) experiment, we developed a two channels 8-Bit 1GHz FADC readout system with RAIN1000Z1 module. With the two R1250 PMTs in the dual end of detector, the analog signals are send to FADC and the digital results is triggered and anticoincidence in the FPGA logic, the final triggered data is send to computer by gigabits Ethernet with ARM processor running Embedded Linux. HMCAD1511 from ADI is used for 8-Bit 1GSPS analog data converter, and the high speed, low jitter 1GHz clock is generated by LMK04803B from TI. With the benefit of high bandwidth and high performance inter connected HP bus between ARM processor (PS) and FPGA logic (PL), the FADC's data gathered by FPGA logic is buffered and transferred to the ARM processor's DDR3 SDRAM running at 1066MHz with CDMA function without many CPU time. The readout interface's data throughput can reach more than 600Mbps with gigabits Ethernet. In this paper, details of the hardware design and HDL design will be introduced.**

I. Introduction

RAIN100Z1 is the high performance readout module we developed last two years [1]. It is based on Xilinx's ZYNQ all programmable SoC (System on Chip), this new architecture integrate the software programmability of a dual core ARM Cortex-A9 processor with the hardware programmability of an FPGA. We have developed a series of readout system based on the RAIN1000Z1 module [2] [3], within the RAIN1000Z1 module, Embedded Linux is running in the ARM processor and real time processing logic is running in the FPGA. Based on the Embedded Linux, TCP/IP socket is used for Ethernet data transport and some slow control software can also be running, such as EPCIS [4].

For the crystal scintillator detectors, we use BC-501A liquid scintillator in a Teflon vessel and the dual R1250 PMT at the left and right end are used to measure the neutron background of CJPL (China Jinping under-ground Lab). To digitalize the signals from 2 PMTs, a new readout electronic system is developed with the RAIN1000Z1 ZYNQ module and Analog to Digital Converter HMCAD1511 from ADI [5]. Fig.1 show the readout electronics system architecture.

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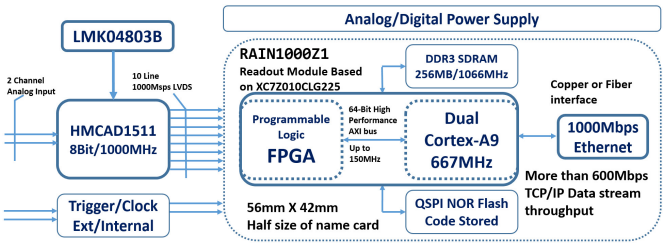

Fig. 1. Readout electronics system architecture.

In Fig.1, the HMCAD1511 is used for digitalization of analog signals from dual R1250 PMT. HMCAD1511 can operate between 3 modes: single channel mode with 1000 MSPS, dual channel mode with 500 MSPS and quad channel mode with 250 MSPS. We use the dual channel mode with 500 MSPS to meet the dual analog signals. In fact there is an integrated cross point analog switch in the analog front of HMCAD1511, no extra circuit is needed to switch in the single channel mode and the dual channel mode. In the test mode, we can change from the dual channel mode to single channel mode to sample only one PMT's analog signal for analysis.

II. Design of Hardware

The HMCAD1511 is easy to use, beside the analog part, it has serial LVDS output to the RAIN1000Z1's FPGA interface. The HMCAD1511 is in the 7×7 mm QFN48 package, it is very small footprint and only 710mW power consumption needed at 1GSPS single channel or 500MSPS dual channel. For thermal consideration, HMCAD1511's QFN48 package's thermal resistance is 29 degree Celsius/W, then the maxim temperature rise is about 20 degree Celsius. With a reasonable PCB thermal pad design for heat dissipation, there is no heatsink needed for HMCAD1511. This is very suitable for compact readout electronics system. For example, we can put ADCs, RAIN1000Z1 module, high voltage power module, power over Ethernet (POE) circuits in a small space such as a PMT base socket.

HMCAD1511 has one differential clock input interface, named CLKP/CLKN. The input differential clock can be supplied in LVDS, LVPECL or sine wave with AC coupled internally. For LVDS or LVPECL clock signals, terminal

resister of 100 Ohm must be placed as close as possible to the clock pins. For sine wave clock input, the amplitude must be least 0.8Vpp, the antiparallel Schottky back to back RF diodes across clock pins can be used to limit clock excursion into the HMCAD1511 to approximately 0.8Vpp differential. In fact, the diode HSMS286C from Avago is used for limit clock signal excursions. This limit helps prevent the large voltage swings of clock from feeding through to other portions of HMCAD1511 while preserving the fast rise and fall times of signal that are critical to arching low jitter performance. But the most important thing is that the diode capacitance comes into play at frequencies above 500MHz, care must be taken in choosing the signal limiting diode. For example, HSMS286C has a typical capacitance about 0.25pF but HSMS2812 is about 1.2pF, and HSMS286C is used for us.

HMCAD1511 has 8 channel of LVDS data outputs, named as DP1A/DN1A, DP1B/DN1B to DP4A/DN4A, DP4B/DN4B, DPxA/DNxA is a couple of LVDS signals. Fig.2 show the dual channel mode data output timing.

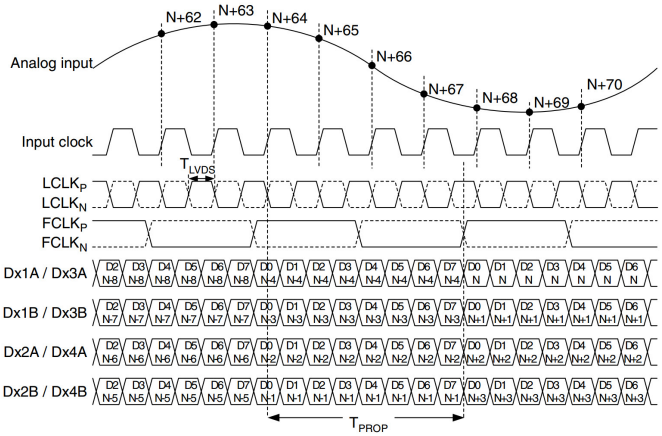

Fig. 2. Dual channel mode data output timing of HMCAD1511.

In Fig.2, input clock is 500MHz for dual channel mode working at 500MHz/8-Bit sampling. LCKP/LCLKN is the LVDS bit clock positive and negative while FCLKP/FCLKN is the LVDS frame clock. In our application of dual channel mode, LCLK is the same frequency to input clock, 500MHz, and FCLK is fourth of input clock, 125MHz.

Typically Giga hertz ADCs use both rise and fall edges to generate internal timing signals, in HMCAD1511 only the rising edge of input clock is used. In Fig.2, every rising edge of input clock, dual input analog signals are sampled. But for the output LCLK, both rise and fall edges are used, output data fetched in both edges. Dx1A/Dx1B, Dx2A/Dx2B are used for first channel of analog input and Dx3A/Dx3B, Dx4A/Dx4B are used for second channel of analog input. Every LVDS couple's data rate is 1GSPS in DDR mode.

HMCAD1511 can be configured by a serial interface, it is very similar to the SPI interface. All of the internal configuration registers can be reached by this interface.

The power supply of HMCAD1511 is split to analog supply, digital supply and digital CMOS input supply. All of these supply is 1.8V normally beside digital CMOS input supply can be 1.8V to 3.3V, but the analog 1.8V should be supply with low noise voltage regulator. We use TPS62130 as DC/DC switch voltage supply to generate 2.1V middle voltage, and use TPS7A7300 to generate low noise 1.8V analog supply from the 2.1V. The ferrite bead BLM21PG331SN1D is also used as RF ripple blocker. It has 1500mA rated current and 330 Ohm impedance at 100MHz.

The analog input of HMCAD1511 is fully differential input, a high speed differential op amplifier is used for single ended signal to differential. LMH6554 from TI is used for ADC driver. At the same time LMH6559 high speed buffer and LMH6702 high speed op amplifier is used in the PMT side to buffer the analog signal to transmit with about 2 meter cable to readout electronics, correspond positive and negative analog low noise power supply is also implemented. Fig.3 show the ADC analog input driver circuit.

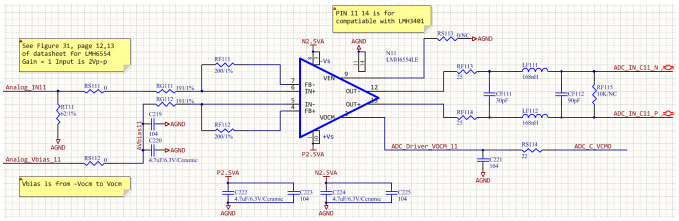

Fig. 3. Block diagram of ADC input driver circuit.

A four channel 16-Bit precision DAC AD5686RBRUZ is used for analog input offset control and high voltage power control, it has the internal 2.5V voltage reference and easy to use SPI interface connected to RAIN1000Z1 module.

III. Software Development

The software design include two section, one is the program design based on C program which is running in embedded Linux and the other one is the logic design based on Verilog program for FPGA also within ZYNQ which is used to design the real time process running in the programmable logic. Fig.4 show the FPGA design flow:

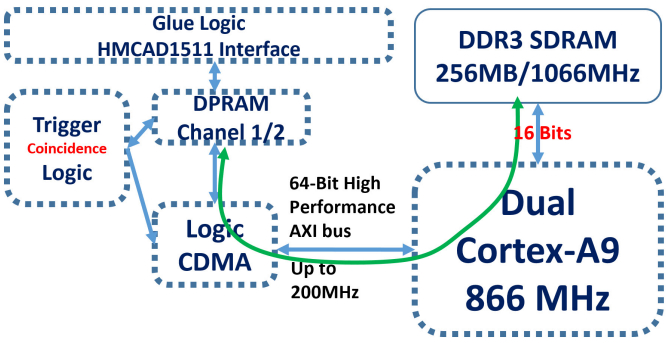

Fig. 4. Block diagram of Verilog program in FPGA.

With the LVDS interface to HMCAD1511, a glue logic is used to fetch and buffer the data flow from ADC to the internal dual port ram (DPRAM), and in our application, it acts as a dual ring buffer to save dual channel data from two analog channel correspond to each PMT.

The trigger and anticoincidence logic monitor the two channel's data and calculate to generate the real time trigger signal. When a valid trigger is send to the CDMA logic, a direct memory access (DMA) is started and the valid event data is fetch to DDR3 SDRAM memory of ARM processor. The embedded Linux will then send data through Ethernet interface to PC. The C program in Linux is not complex, it is based on the socket program of TCP/IP, very easy to handle. The peek data throughput of Giga bit Ethernet is more than 600Mbps.

IV. Test Result

The system's bottle neck is the bandwidth between processor system (PS) to the program logic (PL) and the bandwidth between PS to its DDR3 SDRAM. There are 4 high speed, high performance data path between PS and PL, which is called HP0 to HP3. These 4 data channels support 64-Bit/200MHz operation and can reach 1600MB/s bandwidth; but the 16-Bit/1066MHz SDRAM bandwidth is 1066MB/s for read and write at same time. This is limited by the RAIN1000Z1's 16-Bit data bus design with DDR3 SDRAM.

In our test, when the clock between PS and PL reach to 125MHz (less than the maxim 200MHz), the data rate between DPRAM and DDR3 SDRAM will reach the bottle neck about 810MB/s, it is about 80% of 1066MB/s DDR3 SDRAM data rate, and it is reasonable because the Embedded Linux will use some data bandwidth for OS running.

The sine wave signal generator, SMA100A and specified narrow band filter module is used for test HMCAD1511's ADC performance, and the ENOB is more than 7.5 bits in our system.

Acknowledgment

The new architecture of readout module RAIN1000Z1 based on ZYNQ XC7Z010 in CLG-225 package is compact, with the HMCAD1511 running at 2 channel/500MHz or 1 channel/1000MHz, the readout system is very easy to implement. The Ethernet data throughput is more than 600Mbps, enough for read crystal scintillator detector's data out for neutron monitor.

Next generation of readout module based on XC7Z020 CLG400 footprint is in developing, the DDR3 SDRAM data bus will be expanded to 32-Bit, and the data rate bottle neck will be resolved in future. Data throughput between ADC to DDR3 SDRAM will be upgraded to 1600MB/s, only be limited to silicon chip's speed.

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