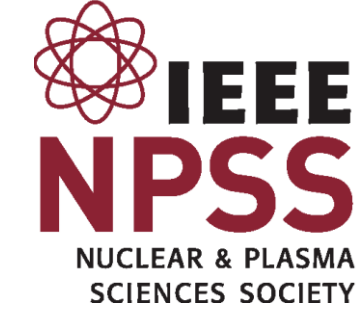




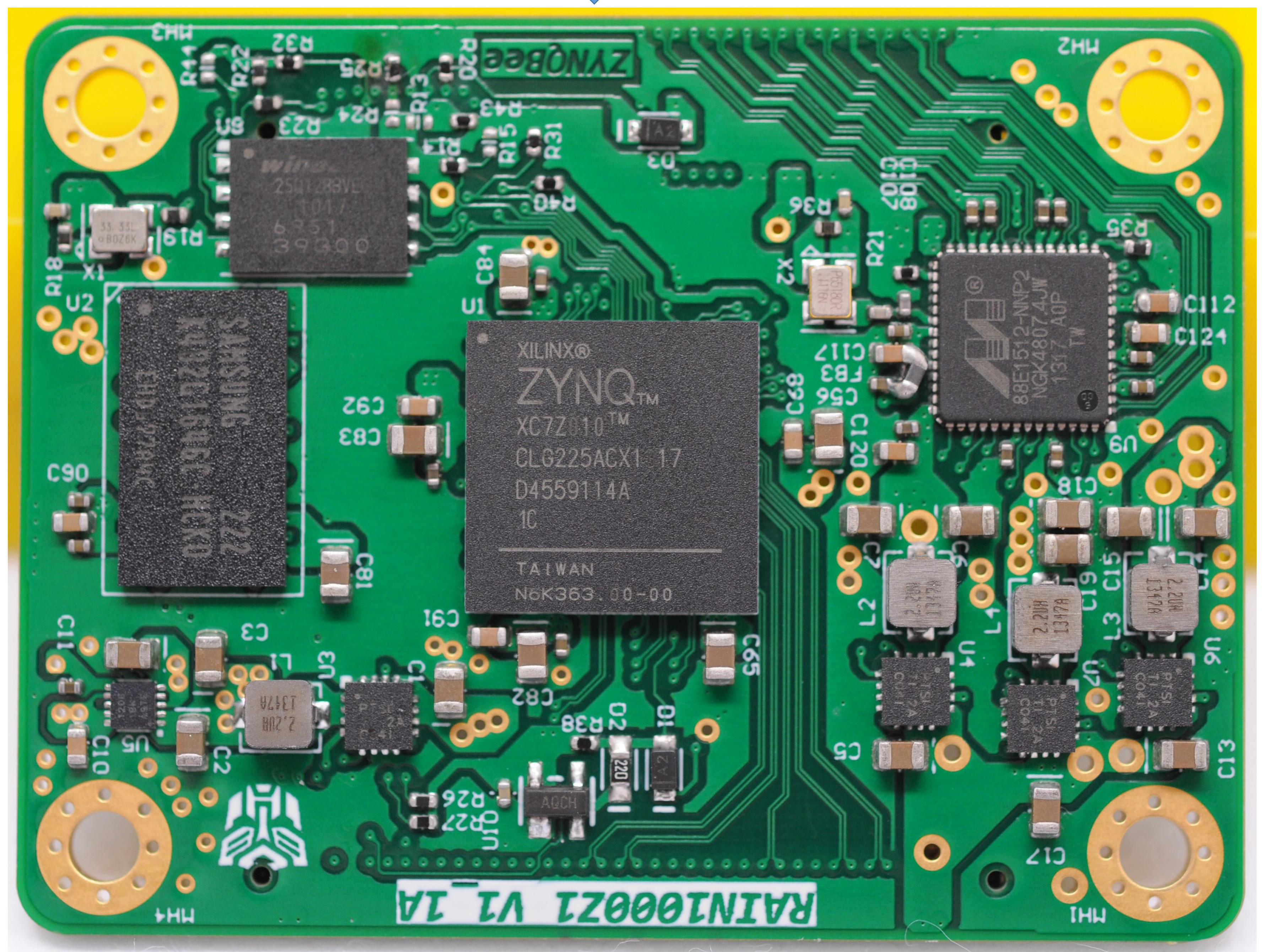
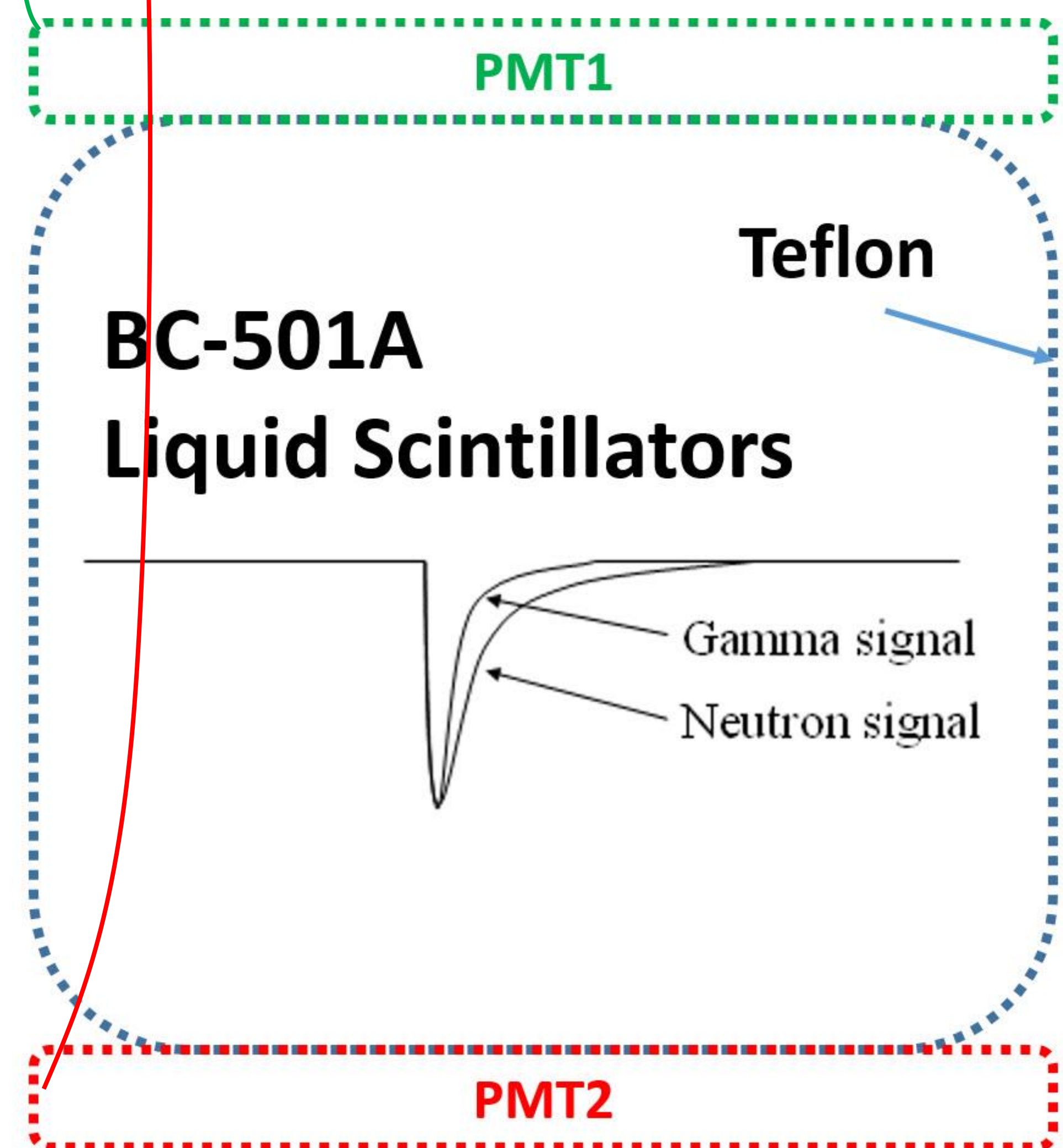
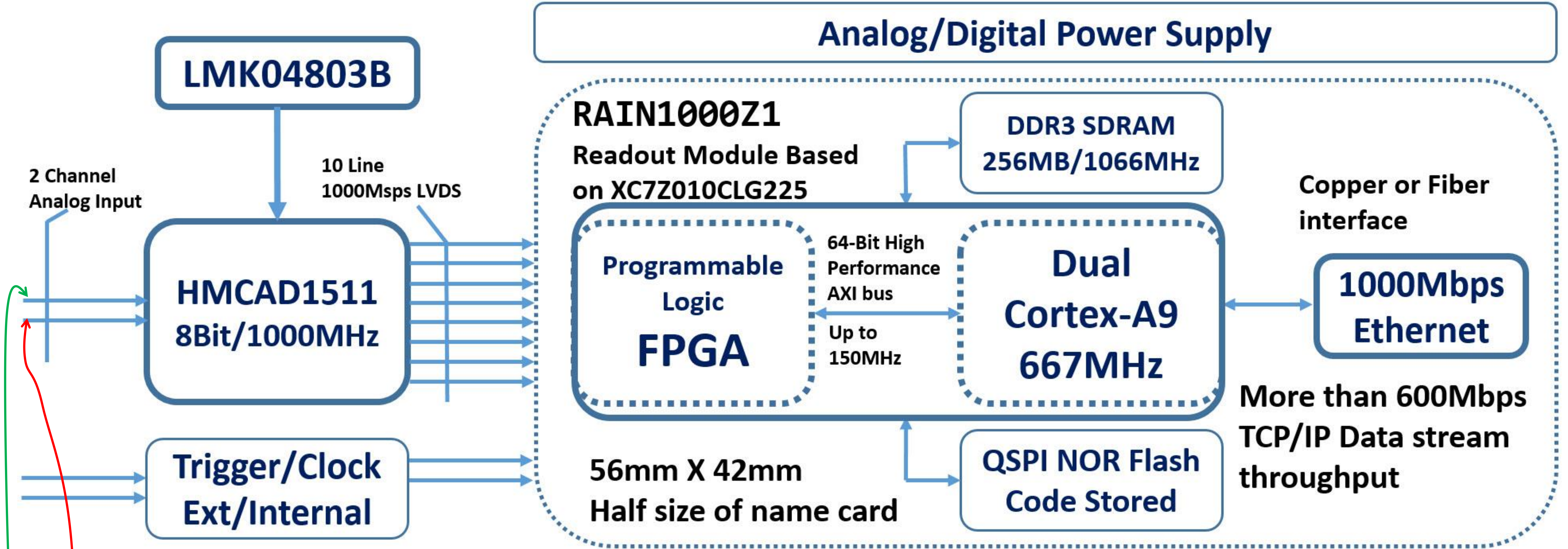
# Readout System with 2-Channel 8-Bit 1GHz FADC Based on RAIN1000Z1 ZYNQ Module for Crystal Detector



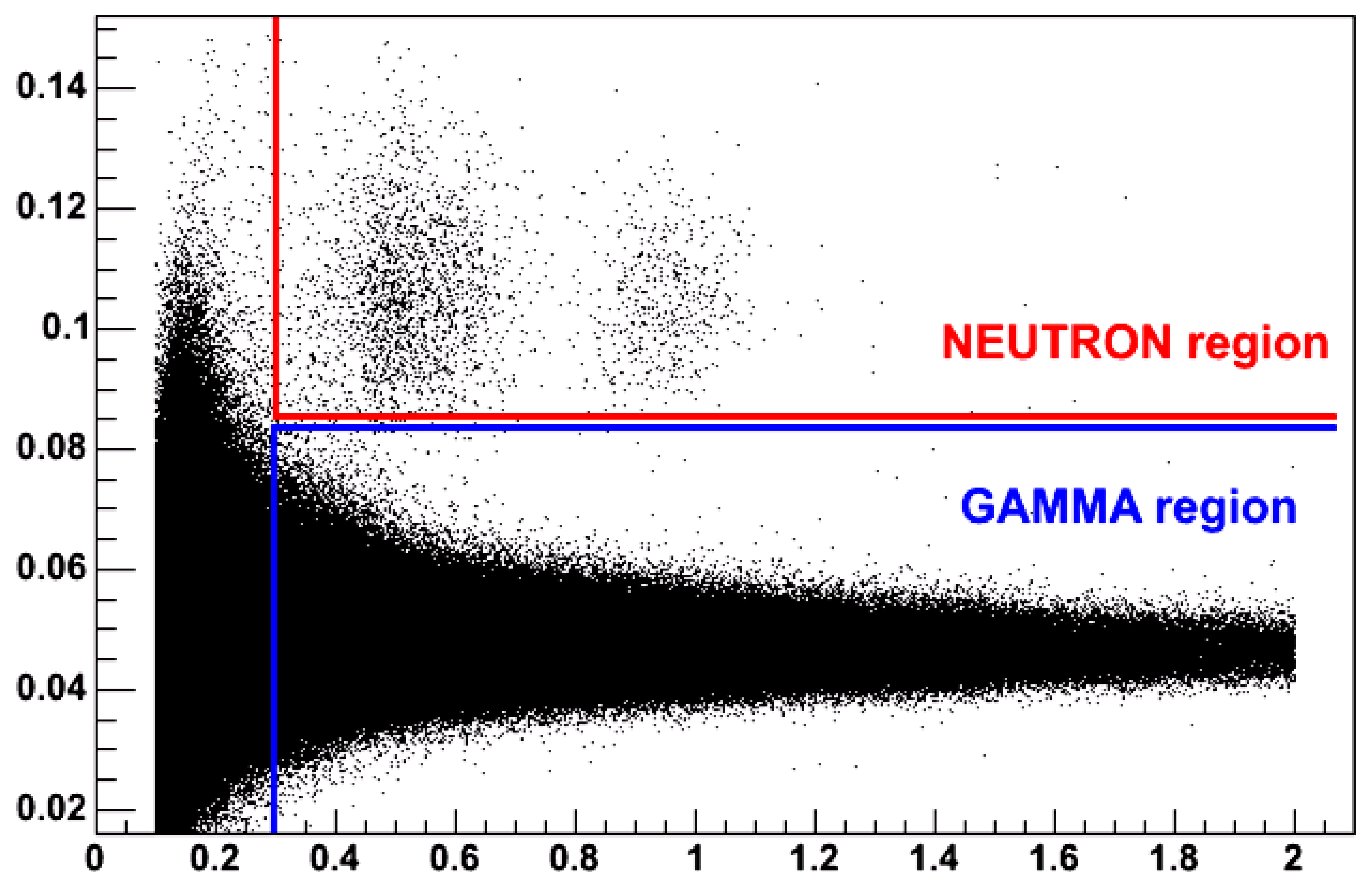
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In SuperK @ 2006



- RAIN1000Z1 is a high performance readout module we developed last two years. It is based on the ZYNQ architecture SOC chip from Xilinx and ZYNQ is the new architecture of FPGA with dual high performance ARM Cortex-A9 processors and high-capacity programmable logic.
- For the liquid scintillator crystal detectors, such as BC-501A, we used for neutron background measurement in the CJPL (China Jinping Underground Lab) experiment hall, we developed a 2-channels 8-Bit 1GHz FADC readout system with RAIN1000Z1 module.
- With the two PMTs in the dual end of detector, the analog signal is send to FADC and the digital results is triggered and anticoincidence in the FPGA logic, the final data is send to computer by gigabits Ethernet with ARM processor running Embedded Linux.
- With the benefit of high bandwidth and high performance inter connected HP bus between ARM processor (PS) and FPGA logic (PL), the FADC's data gathered by FPGA logic is buffered and transferred to the ARM processor's DDR3 SDRAM running at 1066MHz with CDMA function without many CPU time. The readout interface's data throughput can reach more than 600Mbps with gigabits Ethernet.



X is energy of particles and Y is the ratio of signal tail integral VS signal integral  
Threshold is 300keV



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