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Timing distribution and Data Flow for the ATLAS Tile Calorimeter Phase II Upgrade

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The Hadronic Tile Calorimeter (TileCal) detector is one of the several subsystems composing the ATLAS experiment at
the Large Hadron Collider (LHC). The LHC upgrade program plans an increase of order five times the LHC nominal
instantaneous luminosity culminating in the High Luminosity LHC (HL-LHC). In order to accommodate the detector to
the new HL-LHC parameters, the TileCal read out electronics is being redesigned introducing a new read out strategy
with a full-digital trigger system.

In the new read out architecture, the front-end electronics allocates the MainBoards and the DaughterBoards. The
MainBoard digitizes the analog signals coming from the PhotoMultiplier Tubes (PMTs), provides integrated data for
minimum bias monitoring and includes electronics for PMT calibration. The DaughterBoard receives and distributes
Detector Control System (DCS) commands, clock and timing commands to the rest of the elements of the front-end
electronics, as well as, collects and transmits the digitized data to the back-end electronics at the LHC frequency
(˜25 ns).

The TileCal PreProcessor (TilePPr) is the first element of the back-end electronics. It receives and stores the digitized data from the DaughterBoards in pipeline memories to cope with the latencies and rates specified in the
new ATLAS DAQ architecture. The TilePPr interfaces between the data acquisition, trigger and control systems and the
front-end electronics. In addition, the TilePPr distributes the clock and timing commands to the front-end electronics for synchronization with the LHC clock with fixed and deterministic latency.

The complete new read out architecture is being evaluated in a Demonstrator system in several Test Beam campaigns
during 2015 and 2016. At the end of this year, a complete TileCal module with the upgraded electronics will be
inserted in the ATLAS detector.

This contribution shows a detailed description of the timing distribution and data flow in the new read out architecture for the TileCal Phase II Upgrade and presents the status of the hardware and firmware developments of
the upgraded front-end and back-end electronics and preliminary results of the TileCal demonstrator program.

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