Timing Distribution and Data Flow for the ATLAS Tile Calorimeter Phase II Upgrade

F. Carrió, on behalf of the ATLAS Tile Calorimeter System

***Abstract*– The Tile Calorimeter (TileCal) is the hadronic calorimeter covering the central region of the ATLAS experiment at the Large Hadron Collider (LHC). The upgraded High Luminosity LHC will deliver five times the current nominal instantaneous luminosity. The ATLAS Phase II upgrade will upgrade the readout electronics of the TileCal for the HL-LHC. The majority of the front- and back- end electronics will be redesigned with a new readout strategy.**

In the upgraded readout architecture for Phase II, the front-end electronics consist of the Front-End Boards, Main Boards and the Daughter Boards. The Main Board digitizes the analog signals coming from the Front-End Boards (FEBs) connected to the PhotoMultiplier Tubes (PMTs), provides integrated data for minimum bias monitoring and includes electronics for PMT calibration. Three different FEB options with different signal acquisition strategies are under study: new 3-in-1 cards, QIE chip and FATALIC chip. The Daughter Board receives and distributes Detector Control System commands, clock and timing commands to the rest of the elements of the front-end electronics, as well as collects and transmits the digitized data to the back-end electronics at the LHC frequency (~25 ns).

In the back-end electronics, the TileCal PreProcessor (TilePPr) receives and stores the digitized data from the Daughter Boards in pipeline memories to cope with the latencies and rates specified in the new ATLAS DAQ architecture. The TilePPr interfaces between the data acquisition, trigger and control systems and the front-end electronics. In addition, the TilePPr distributes the clock and timing commands to the front-end electronics for synchronization with the LHC clock.

I. Introduction

THE Tile Calorimeter (TileCal) [1] is the hadronic calorimeter of the ATLAS [2] experiment at the Large Hadron Collider (LHC) at CERN. TileCal is a sampling detector using steel plates as absorber and plastic scintillator tiles as active material; it covers the central part of the ATLAS experiment. This detector is divided into four sections along the beam direction, each of which is segmented azimuthally into 64 modules (Figure 1a). The Photomultiplier Tubes (PMTs) and the front-end electronics are located in mechanical structures called "drawers", placed in the outermost part of the modules (Figure 1b). The complete readout of the TileCal cells comprises a total of 9852 PMTs.

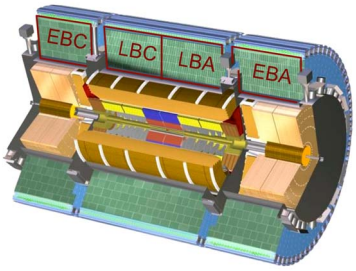

Fig. 1a. Tile Calorimeter detector.

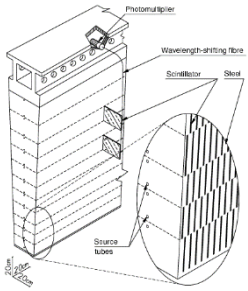

Fig. 1b. Tile Calorimeter module.

II. Current Readout Architecture

In the present front-end electronics, the analog signals produced by PMTs are conditioned and amplified in the 3-in-1 cards with two gains, and digitized by the Digitizer chips at the LHC frequency. The digitized data are stored in pipelined memories in the Digitizers until the reception of a Level-1 trigger acceptance signal (L1A). When an L1A signal is received, the Interface Board collects the selected events and sends them to the ReadOut Drivers (RODs) [3] in the back-end electronics through a dedicated optical link. RODs are responsible of processing the incoming data at a maximum average rate of 100 kHz.

Parallel to this process, the analog signals coming from the 3-in-1 cards are analog summed in towers every bunch crossing and transmitted to the Level 1 Calorimeter trigger system (L1Calo) for the selection of potentially interesting events. Figure 2 shows the data flow of the TileCal architecture.

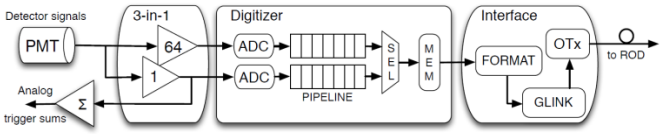

Fig. 2. Diagram of the current readout architecture of the Tile Calorimeter.

F. Carrió is with the Instituto de Física Corpuscular (CSIC-UV), Catedrático José Beltrán 2, Paterna, Spain (e-mail: Fernando.carrio @cern.ch).

III. Phase II upgrade readout architecture

After the ATLAS Phase II Upgrade [4] in 2027, the High Luminosity LHC (HL-LHC) will deliver a nominal instantaneous luminosity of 5-7·10^{34} $cm^{-2}s^{-1}$ with a pileup close to 200 events per bunch crossing providing a total integrated luminosity of 3000 fb^{-1} in ten years.

The Phase II Upgrade requirements make necessary a full redesign and replacement of the readout architecture and trigger systems to improve the event selections and cope with the new radiation levels, latency and high data rates.

Figure 3 shows a diagram of the readout architecture for the ATLAS Tile Calorimeter Phase II Upgrade. The new readout architecture requires a fully digital trigger system where the front-end electronics will transmit all the digitized samples to the Tile PreProcessors (TilePPr) in the back-end electronics at the LHC frequency.

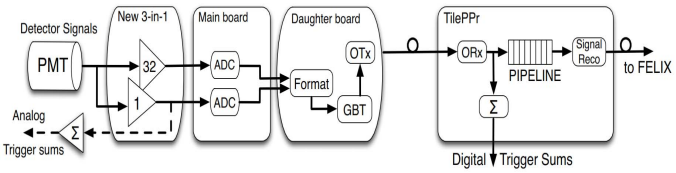

Figure 3. Diagram of the TileCal Phase-II Upgrade readout electronics.

Table 1 shows a comparison between the data bandwidth requirements for the current readout system and for the Phase II Upgrade readout system.

TABLE I. TILE CALORIMETER READOUT FEATURES COMPARISON

	Current	Phase II Upgrade
Total BW	205 Gbps	40 Tbps
N. fibers	256	4095
BW/module	800 Mbps	160 Gbps
Nb. boards	32	32
Nb. crates	4 (VME)	4 (ATCA)
In BW/board	6.4 Gbps	1.28 Tbps
Out BW/board$_{DAQ}$	2.56 Gbps	40 Gbps
Out BW/board$_{L1/L0}$	Analog	500 Gbps

IV. The Tile Calorimeter Demonstrator Project

The Demonstrator Project aims to evaluate and qualify the proposed readout architecture before its full replacement during the Long Shutdown 3 (2024-2027). As part of the Demonstrator activities the new system is being validated in several Test Beam campaigns at CERN during 2015 and 2016. It is hoped that at the end of 2016 a complete TileCal module with the upgraded electronics will be inserted in the ATLAS detector.

The Demonstrator module comprises on a single frame, the front-end upgraded electronics needed for the digitization of signals coming from the PMTs, the calibration circuitry and high speed data communication with the back-end electronics, and the electronics needed for the distribution and monitoring of high voltage to the PMTs. Since the full digital trigger system will not be present until Phase II, the Demonstrator module will also provide analog trigger signals to the current L1Calo system.

V. Upgraded front-end electronics

A. Front-end boards

Three different FEB options are being evaluated for the ATLAS Phase II Upgrade. The first FEB option is an improved version of the current 3-in-1 card [5] used in TileCal. This FEB has been designed using Commercial Off-The-Shelf components and provides analog outputs with two different gains, as well as calibration capabilities for PMTs. The new 3-in-1 card shows better linearity and lower noise and has passed successfully the radiation certification. The modified 3-in-1 card has been chosen as FEB for the Demonstrator module, since it is the only FEB providing analog outputs required for the current trigger system.

The second option is a custom ASIC called Charge Integrator and Encoder (QIE) [6]. This ASIC divides the signal coming from the PMTs with a current splitter followed by a gated integrator providing four different ranges (16/23, 4/23, 2/23, 1/23). In the same chip, a 6-bit flash ADC digitizes the selected range covering a dynamic range of 17 bits.

The third option for the FEB is a mixed ASIC called Front-end for ATLAS TileCal Integrated Circuit (FATALIC) [7]. FATALIC includes analog and digital processing blocks. A current conveyor connected to three shaping stages with different gains covers the full dynamic range of the PMT signal. The conditioned signals are digitized using three 12-bit ADCs also present in the ASIC, and stored in a pipelined memory. A digital processing block performs the auto-selection between low- and high-gain data and transmits the auto-selected and the medium gain data through a high speed serial link.

B. Main Board

The Main Board interfaces the Daughter Board and the FEBs. It is responsible for the control, monitoring and readout of the FEBs.

TileCal modules will include four Main Boards, where one Main Board will host and manage up to 12 FEBs. Three different types of Main Board will be designed in order to accommodate the three FEB options.

A Main Board capable to accommodate and operate up to 12 new 3-in-1 cards has been designed for the Demonstrator module. This board includes four Altera Cyclone IV FPGAs to control and to configure the FEBs, while 12-bit ADCs digitize the analog shaped signals coming from the new 3-in-1 cards.

Each half of the Main Board is powered with a separate low voltage power supply, where power connections from one half are diode-ORed with the other half. Figure 4 shows a picture of the Main Board prototype for the Demonstrator.

978-1-5090-2014-0/16/$31.00 ©2016 IEEE

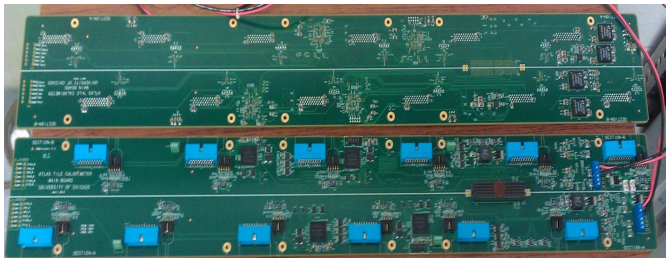

Fig. 4. Photograph of the Main Board.

C. Daughter Board

The Daughter Board [8] is the interface between the front- and back-end electronics. The Daughter Board receives and deserialize low- and high-gain data samples from the 12 FEBs connected to the Main Board at the LHC frequency. Sampled data is packed and transmitted to the back-end electronics using redundant high speed links at data rates of 9.6 Gbps.

The Daughter Board used in the Demonstrator includes two Xilinx Kintex 7 FPGAs, two Quad Small Form-factor Pluggable (QSFP) optical modules, two GBTx [9] chips and an FPGA Mezzanine Connector (FMC) for the communication with the Main Board. Figure 5 shows a picture of the Daughter Board version 4.

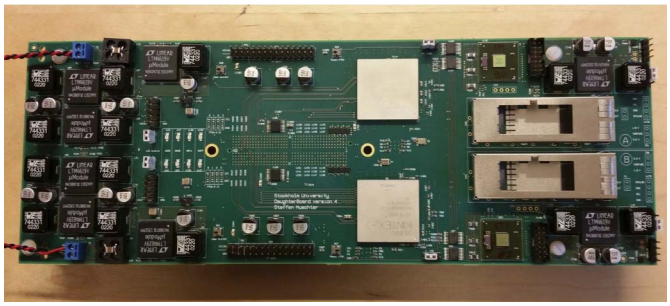

Fig. 5. Photograph of the Daughter Board version 4.

VI. Upgraded Back-End Electronics

The TilePPr will be the main component of the back-end electronics after the ATLAS Phase II Upgrade. This module will provide a high speed link for the readout, operation and monitoring of the front-end electronics. Moreover, the TilePPr will send calibrated information to the ATLAS trigger systems with improved granularity and precision.

High speed links will distribute the Trigger, Timing and Control (TTC) information and the Detector Control System (DCS) commands towards the TileCal front-end electronics.

The TilePPr will be designed in an ATCA [10] form factor, where each TilePPr will manage up to eight TileCal modules, each one containing up to 48 PMTs. A total of 32 TilePPr will be required for the complete readout of the TileCal detector.

A Rear Transition Module (RTM) called TDAQ-I, will interface the TilePPr with the ATLAS trigger and data acquisition (TDAQ) readout system.

The TDAQ-I will receive event data from the TilePPr every bunch crossing and will transmit preprocessed trigger information to the calorimeter and muon trigger systems at the LHC frequency.

For every bunch crossing, the TilePPr boards will receive, decode and store event data in circular pipeline memories, until the reception of a trigger acceptance signal. The selected data will be transmitted to the Front End LInk eXchange [11] (FELIX) system, for proper event data decoding and transmission to the next trigger level.

Figure 6 shows a preliminary diagram of the TilePPr for Phase II Upgrade.

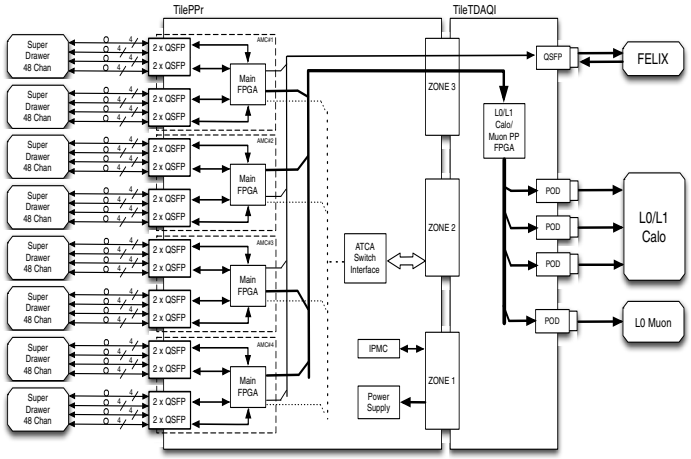

Fig. 6. Diagram of the TilePPr for Phase II Upgrade.

A. The TilePPr prototype

The TilePPr prototype [12] has been designed and produced in the framework of the Demonstrator Project. The TilePPr demonstrator is responsible for the reception, processing of the digital data coming from the Demonstrator module, as well as for the distribution to the front-end electronics of TTC data for synchronization with the LHC clock. It represents one eight of the final TilePPr board.

The TilePPr prototype has been designed as a double mid-size Advanced Mezzanine Card (AMC) and is populated with 4 QSFPs connected to a Virtex 7 FPGA, one Kintex 7 FPGA, two Avago MiniPOD modules (one transmitter and one receiver), DDR3 memories and jitter cleaners. Figure 7 shows a picture of the TilePPr demonstrator.

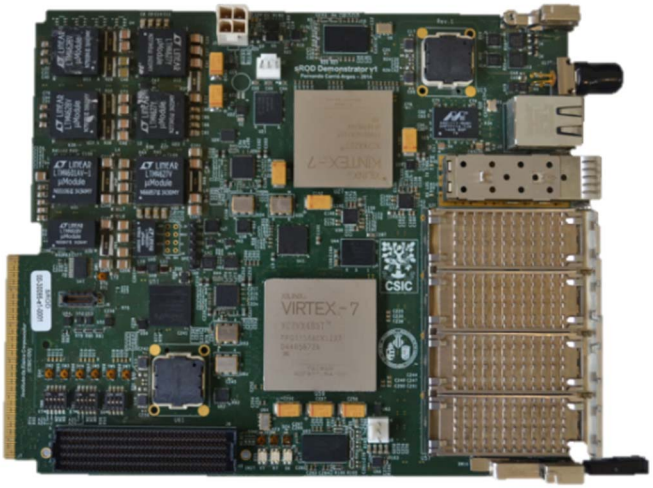

Fig. 7. Photograph of the TilePPr prototype.

The high speed communication path between the front-end and back-end electronics is implemented through 16 GigaBit Transceiver (GBT) [13] links at 4.8 Gbps for the downlink

(TilePPr to front-end electronics) and 9.6 Gbps for the uplink (front-end electronics to TilePPr).

The downlink is used to send DCS and TTC commands at the standard data rate of the GBT protocol (4.8 Gbps) with Forward Error Correction (FEC). Each Daughter Board receives 4 GBT links, with one link connected to a GBTx chip for clock recovery and remote configuration and the other three links connected to the Kintex 7 FPGAs for command reception and clock distribution to the Main Board.

In the uplink, the GBT firmware has been adapted to operate at 9.6 Gbps in order to have enough data bandwidth to read out all the channels of the Demonstrator module every bunch crossing. The received data is stored in pipeline memories upon the reception of a L1A when the data is packed and transmitted to the FELIX prototype system and to the present RODs, thus providing compatibility between the current architecture and the Demonstrator module.

In order to achieve synchronous communication between the front-end and the back-end electronics at the LHC frequency, the TilePPr recovers the LHC clock from the TTC stream and cleans it with a jitter cleaner reducing the jitter levels up to the required values for error-free data transmission.

VII. Conclusions

A new readout architecture with a fully digital trigger will be implemented to fulfill the new requirements of the HL-LHC during the ATLAS Phase II Upgrade. The increase of the radiation levels and the larger data bandwidth implies the complete redesign of the front-end and back-end electronics of Tilecal.

This contribution shows a description of the data flow and timing distribution in the new readout architecture for the TileCal Phase II Upgrade and presents the status of the hardware and firmware developments of the upgraded front-end and back-end electronics.

References

[1] ATLAS Collaboration, Readiness of the ATLAS Tile Calorimeter for LHC collisions, Eur. Phys. J. C, 70 (2010).

[2] ATLAS collaboration, The ATLAS Experiment at the CERN Large Hadron Collider, 2008 JINST 3 S08003.

[3] A. Valero et al., ATLAS TileCal Read Out Driver production, 2007 JINST 2 P05003.

[4] ATLAS Collaboration, Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment, CERN-LHCC-2012-022, (2012).

[5] F. Tang et al., Design of the front-end readout electronics for the ATLAS tile calorimeter at the sLHC, IEEE Transactions on Nuclear Science, Vol. 60, NO. 2. 1255-1259, April. 2013.

[6] A Baumbaugh, L Dal Monte, G Drake, J Freeman, D Hare, H Hernandez Rojas, E Hughes, S Los, D Mendez Mendez, J Proudfoot, T Shaw, C Tully, R Vidal, J Whitmore and T Zimmerman, QIE10: a new front-end custom integrated circuit for high-rate experiments, 2014 JINST 9 C01062.

[7] N. Pillet, et al., FATALIC, A wide dynamic range integrated circuit for the Tilecal VFE ATLAS upgrade. TWEPP 2011, 2011.

[8] S. Muschter et al., Development of a digital readout board for the ATLAS Tile Calorimeter upgrade demonstrator, 2014 JINST 9 C01001.

[9] P. Moreira et al., The GBT-SerDes ASIC prototype, 2010 JINST 5 C11022.

[10] PICMG, PICMG 3.0 Revision 3.0 AdvancedTCA Base Specification, March 2008.

[11] J. Anderson et al., FELIX: a High-Throughput Network Approach for Interfacing to Front End Electronics for ATLAS Upgrades, ATL-DAQ-PROC-2015-014, https://cds.cern.ch/record/2016626.

[12] F. Carrió et al., Performance of the Tile PreProcessor Demonstrator for the ATLAS Tile Calorimeter Phase II Upgrade, 2016 JINST 11 C03047.

[13] M. Barros et al., The GBT-FPGA core: features and challenges, 2015 JINST 10 C03021.