



CONSEJO SUPERIOR  
DE INVESTIGACIONES  
CIENTÍFICAS



# Timing distribution and Data Flow for the ATLAS Tile Calorimeter Phase II Upgrade

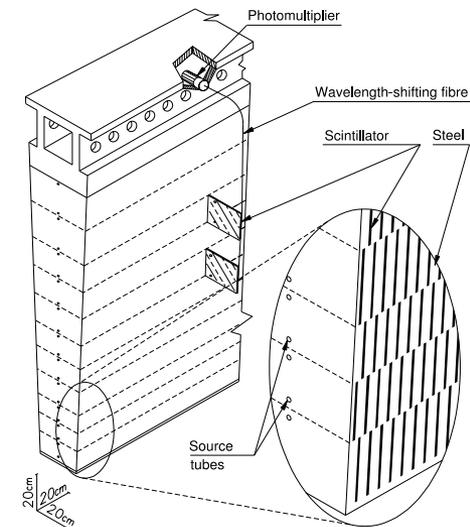
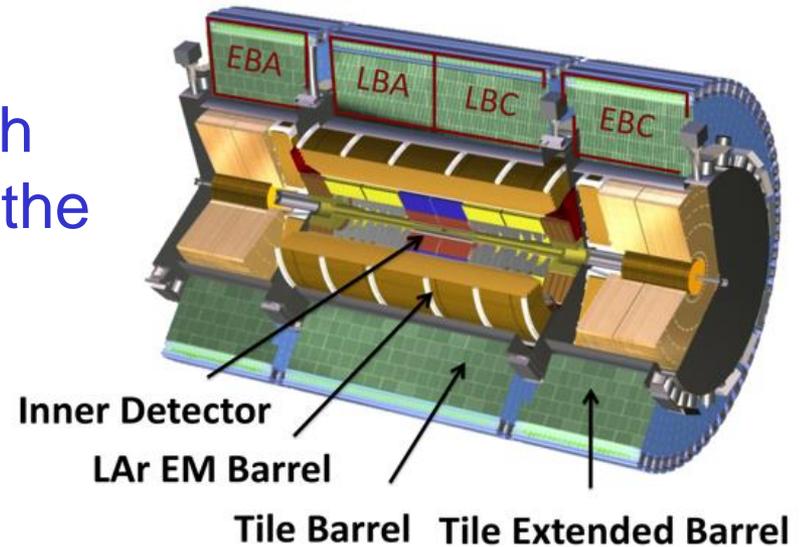


Fernando Carrió Argos on behalf of the ATLAS Tile  
Calorimeter Group



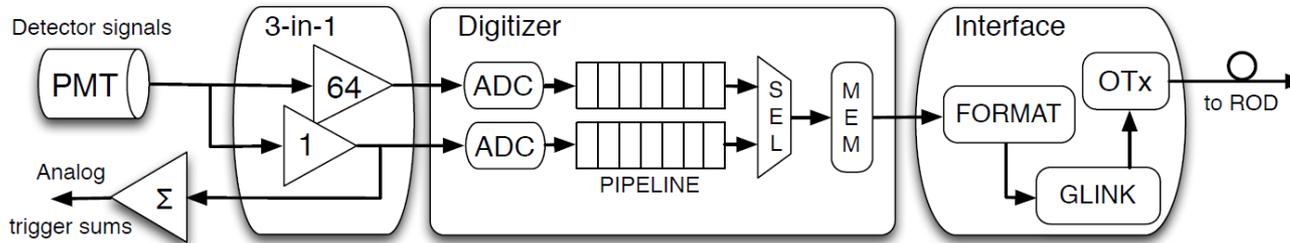


- Segmented calorimeter of steel plates and plastic scintillator which covers the most central region of the ATLAS experiment
  - 4 partitions: EBA, LBA, LBC, EBC
    - Each partition has 64 modules
      - One drawer hosts up to 48 Photo Multiplier Tubes (PMTs)
  - Light produced by a charged particle passing through a plastic scintillating tile is transmitted to the PMTs
  - Signals coming from PMTs are digitized and stored in the front-end electronics upon the reception of a Level-1 accept
  - Around 10,000 readout channels

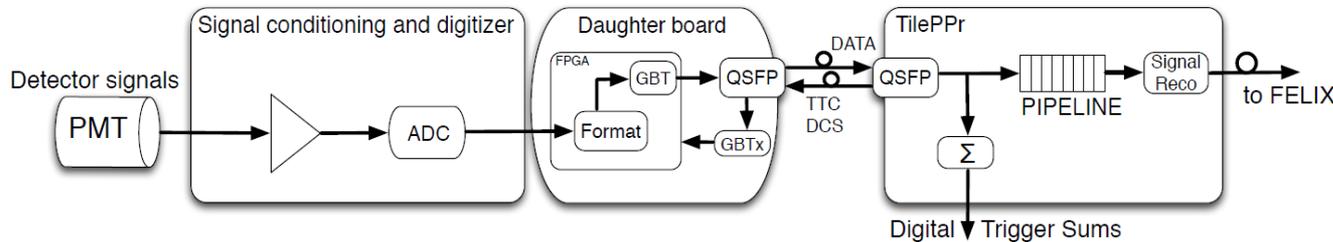




## Present front-end electronics



## Equivalent electronics for phase-II upgrade

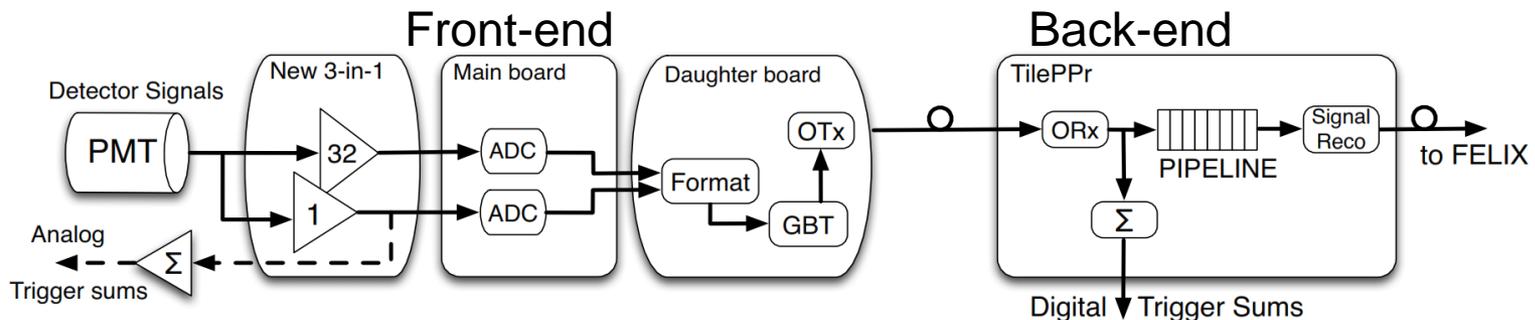


	Present	Phase II
<b>Total BW</b>	~205 Gbps	~40 Tbps
<b>N. Fibers</b>	256	4095
<b>BW/mod.</b>	800 Mbps	160 Gbps
<b>Nb. boards</b>	32	32
<b>Nb. crates</b>	4 (VME)	4 (ATCA)
<b>In BW / board</b>	6.4 Gbps	1.28 Tbps
<b>Out BW / board<sub>DAQ</sub></b>	2.56 Gbps	40 Gbps
<b>Out BW / board<sub>L1/L0</sub></b>	Analog	500 Gbps

- LHC plans to increase the instantaneous luminosity by a factor 5-7 around 2027
- Phase II Upgrade: Major replacement of the readout electronics
  - New readout architecture to provide digital trigger information at low latency for L0/L1 trigger systems with improved granularity
    - Pipelines, de-randomizers memories, TTC distribution moved to the back-end electronics
- Higher radiation tolerance of electronics
- Higher reliability and robustness of electronics reducing single point failures

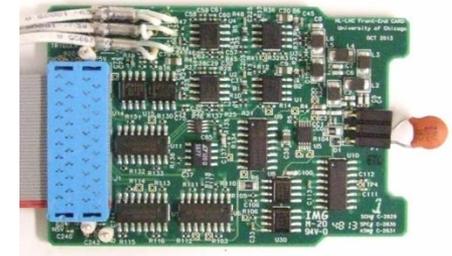


- Evaluation the new readout schema and trigger system interfaces
  - TileCal demonstrator module is operative in our labs at CERN
- Plans for the demonstrator project
  - Test beam in 2015 and 2016
  - Possible insertion of one demonstrator module into the ATLAS at the end of 2016
  - Insertion of more modules during LS2(2019-2020) depending of the demonstrator results and performance
- Readout architecture for Phase II but keeping backward compatibility with the current system
  - Tile PreProcessor will interface the current TTC system (or FELIX) with the new front-end electronics
  - Back-end electronics will send Level 1 selected events to the current RODs
  - Provide analog trigger signals to the present trigger system



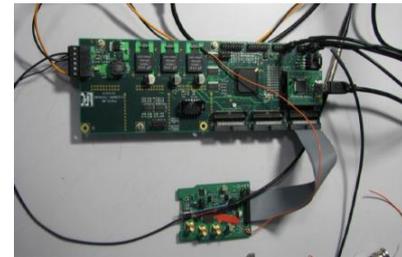


- 3-in-1 Cards: Based on current 3-in-1
  - Provides 3 analog signals: 2 x LG + 1 x HG
  - Calibration circuitry
  - Improved noise and linearity
  - Design ready and qualified
  - **Selected option for the Demonstrator as this option provides analog signals to the current trigger system**

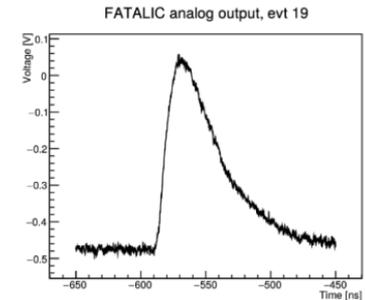


3in1 card

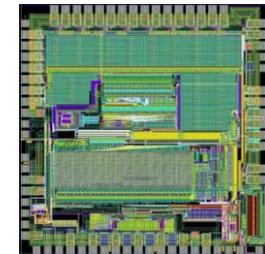
- FATALIC: Combined ASIC solution
  - Current conveyor and three shaping stages
  - 3 different gain ratios (1, 8, 64)
  - Integrated 12-bit pipelined ADCs
  - Tested during the last Test Beam → Shows good performance



FATALIC



- QIE: Charge Integrator and Encoder
  - Current splitter with four ranges and gated integrator
  - 6-bit flash ADC at 40 MHz operation
  - 17 bit dynamic range in 10 bits
  - Integration in a FEB and DAQ development during the Q2 of 2016
  - To be tested during the next Test Beam (June 2016)



QIE chip

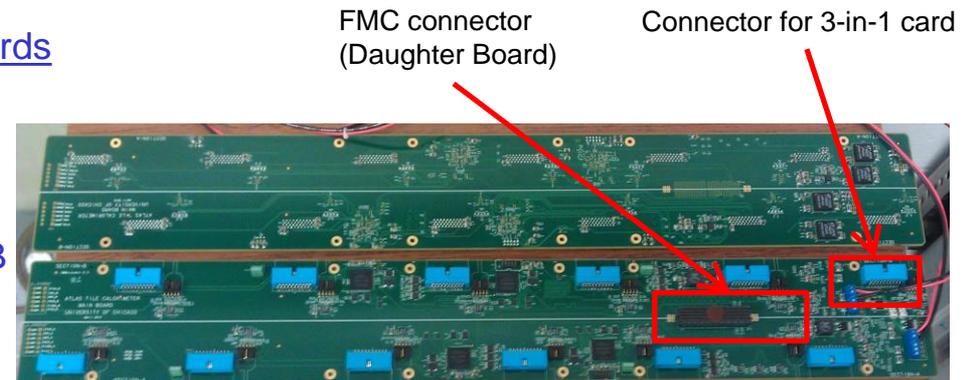


- High speed communication between front- and back-end electronics
  - Reception of timing and control commands
  - Transmission of digitized data to the BE
- Daughter Board v4
  - 2 Xilinx Kintex 7 FPGA
  - 2 QSFP module (2 x 40 Gbps)
  - 2 GBTx chips
    - One GBTx per QSFP+
    - Allows remote programming and operation from the BE



*Daughter Board v4*

- 
- Main Board
    - **Demonstrator** → Version for modified 3-in-1 cards
  - Digitize signals coming from 12 modified 3-in-1 cards
    - 12 bits, 40 MSPs
  - Digital control of the front-end boards using Altera Cyclone IV
  - Routes the digitized data from the ADCs to the DB
    - 400 pin FPGA Mezzanine Connector (FMC)
    - LVDS at 560 Mbps per ADC
  - Low power voltage distribution
    - Divided into two halves for redundancy



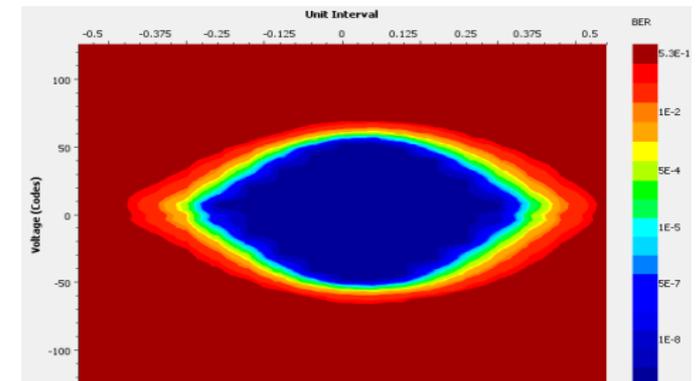
*Main Board for 3-in-1 cards*



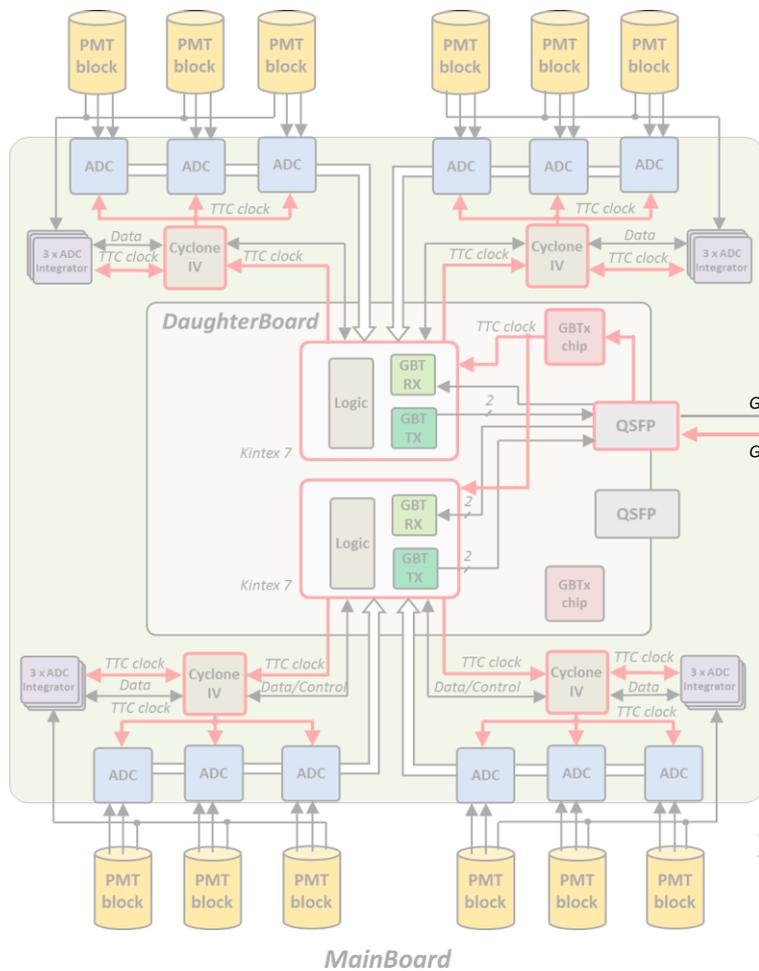
- Represents 1/8 of the final TilePPr module for the ATLAS Phase II Upgrade
- Double mid-size AMC form factor
  - ATCA carrier /  $\mu$ TCA
- Virtex 7 + 4 QSFPs (Readout)
  - Readout and operation of 1 complete TileCal module
  - Timing and command distribution to the FE
  - Interface with FELIX system
  - Energy and time reconstruction algorithms
- Kintex 7 + Avago MiniPOD TX (Trigger)
  - Evaluation of the interfaces with trigger systems and latencies between systems
  - Trigger data preprocessing algorithms
- DDR3 memories, FMC, GbE ports, PCIe, ...
- System has been successfully tested
  - BERT showed no errors during 115 hours
  - $5 \cdot 10^{-17}$  for a confidence level of 95%
  - 16 links at 9.6 Gbps with PRBS31 pattern



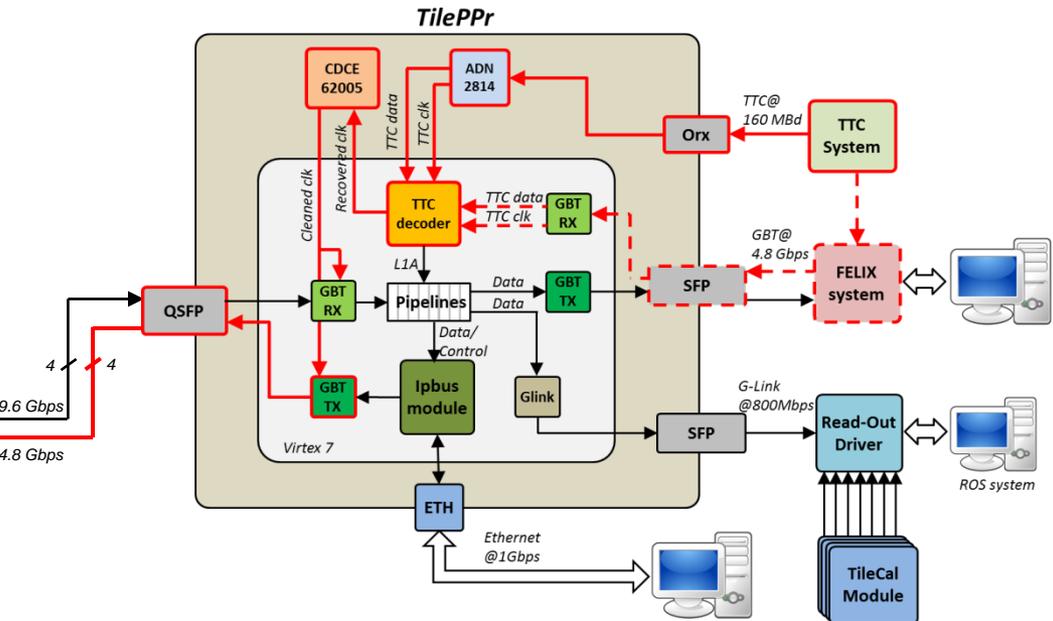
TilePPr prototype



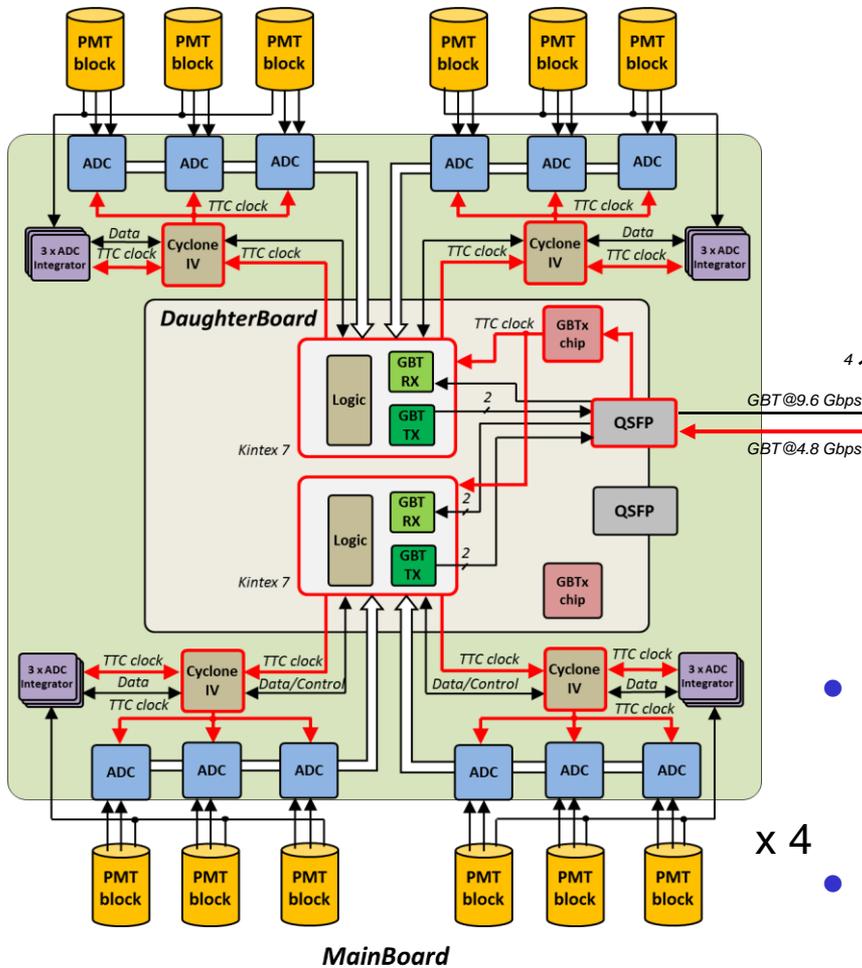
Eye diagram at 9.6 Gbps (GTX)



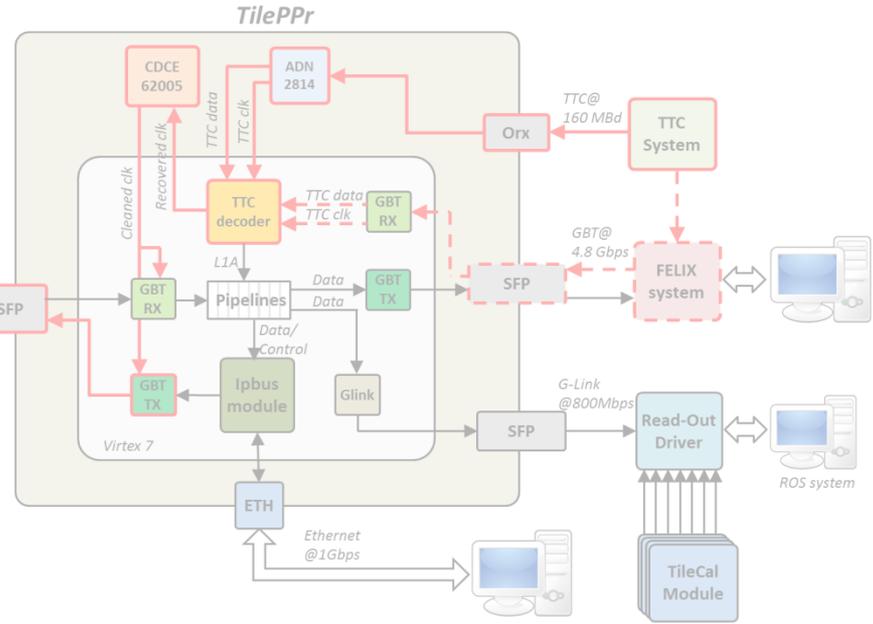
x 4



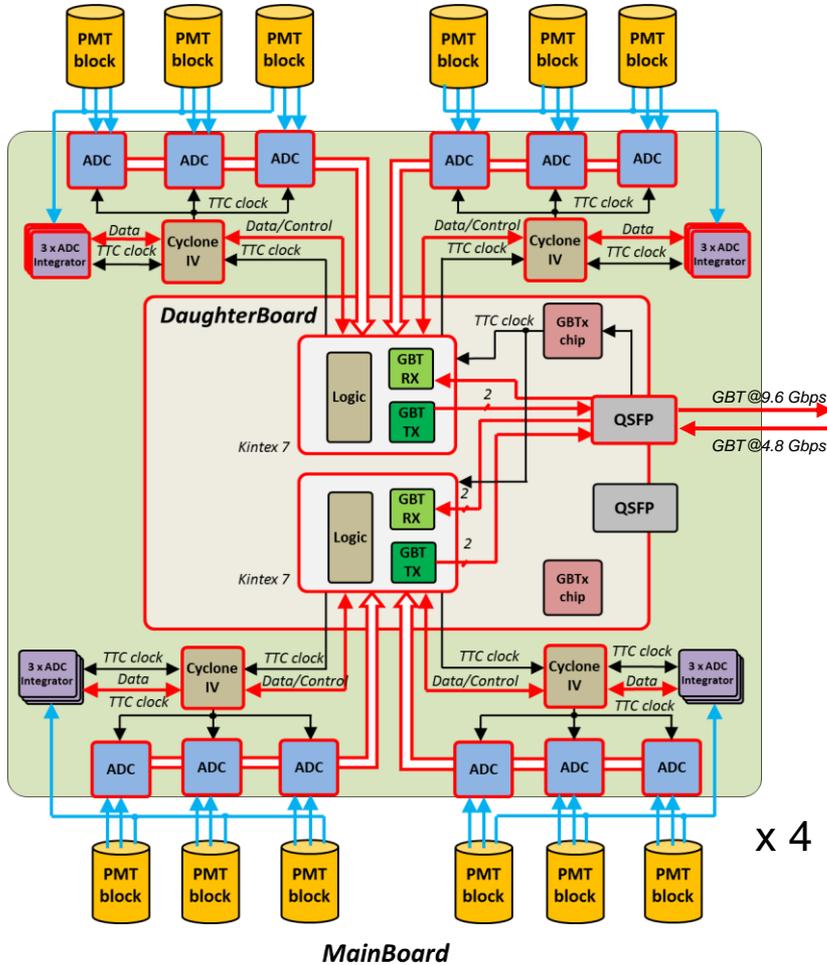
- TTC system provides FE configuration commands, LHC clock, and trigger signals
  - Legacy TTC system: clock is recovered using a dedicated chip (ADN2814)
  - FELIX: clock is recovered through the GTX transceivers (FPGA)
- External jitter cleaners chips are used to improve the quality of the recovered clock
- Clock is sent to the FE embedded with the data/commands
  - Downlink @ 4.8 Gbps, 4 x GBT links
  - Transceivers configured in deterministic and fixed latency mode



x 4



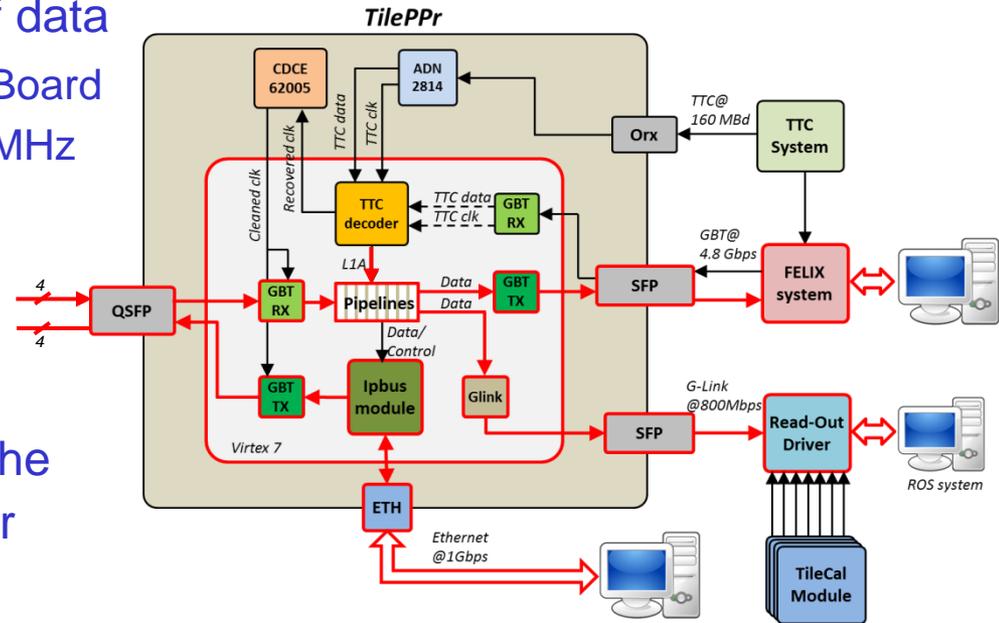
- GBTx chip recovers the LHC clock from one GBT link
  - Clock with deterministic and fixed latency
  - Used for GBT frame decoding in the Kintex 7 FPGAs
  - GBTx chip is also used for remote operation and programming
- Cyclone IV FPGAs distribute the LHC clock to the ADCs for digitization
  - Capability of phase shifting in fine steps
- Commands are received through the other three GBT links in the downlink – 4.8 Gbps



- Front-end electronics transmits the digitized data to the back-end electronics for every bunch crossing
  - 4 GBT links @ 9.6 Gbps
- No memory buffers in the front-end
- Each Kintex 7 FPGAs deserializes the data coming from 6 ADCs at 560 Mbps
- Event data is packed in a GBT frame with other monitoring info (HV, FE status, etc)
- Commands are decoded in the Kintex 7 FPGA and distributed to the MainBoard
  - Front-end boards settings
  - ADC configuration
  - HV electronics configuration
- Analog sums of the low gain signals coming from the PMTs are transmitted to the current trigger system for decision
  - In order to keep backward compatibility with the legacy trigger system

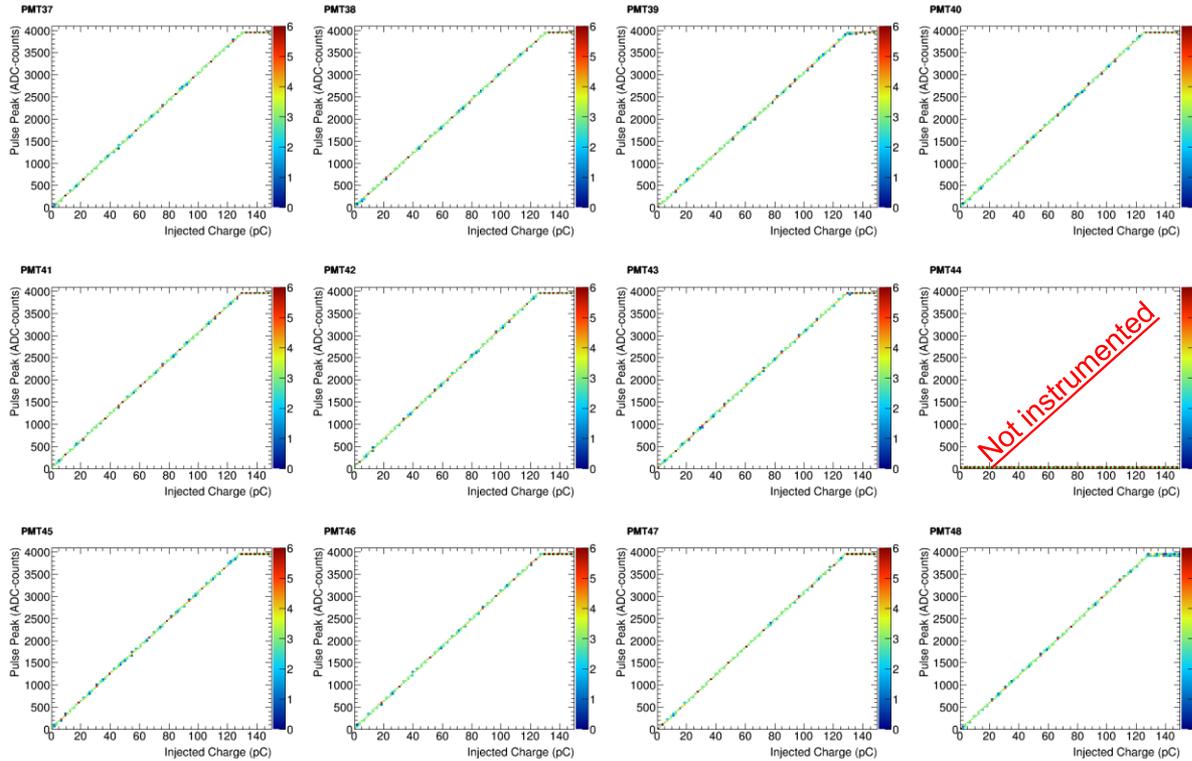


- Continuous decoding and reception of data
  - 4 GBT links @9.6 Gbps per DaughterBoard
  - 12 bits x 12 channels x 2 gains @ 40 MHz
- Data is stored in circular pipelines
  - Samples with 2 gains x 48 channels (1 TileCal module)
  - 12.5  $\mu$ s depth memories
- Selected event data is transmitted to the readout systems after a Level-1 trigger signal is received
- Three independent readout paths
  - FELIX system prototype: Phase II
    - 1 GBT link@4.8Gbps
    - 32 samples x 2 gains @ ~20 kHz
  - Legacy Read-Out Drivers: Backward comp.
    - 1 G-Link@800 MBps
    - 7 samples x 1 gain @100kHz
  - IPbus protocol via Ethernet: Monitoring
    - 32 samples x 2 gains



- Remote control / monitoring
  - Front-end boards configuration
  - High Voltage electronics
  - FPGAs status
  - Temperatures

# Charge injection linearity test





- R&D projects for ATLAS Phase II Upgrade includes the implementation of a new readout architecture:
  - Complete redesign of the front-end and back-end electronics for Phase II Upgrade
  - New trigger and readout strategies with new trigger algorithms
  - No buffers in the front-end electronics → all data will be readout at LHC frequency
  - LHC clock is distributed embedded with the downlink data (GBT@4.8 Gbps)
- Tile Demonstrator electronics project
  - Functional prototypes of front- and back-end electronics
  - Implemented redundancy in all front-end elements
  - Possibility of installing a TileCal demonstrator at the end of this year



**Thank you**