Contribution ID: **76** Type: **Poster presentation**

Online calibration of the TRB3 FPGA TDC with DABC software

Tuesday 7 June 2016 15:00 (1h 30m)

The *TRB3* - Trigger Readout Board - features 4 FPGA based TDCs with a total of up to 264 channels and a time precision of 8 ps RMS **[1]**. It was applied for various beam tests and is going to serve as a standard DAQ hardware for *FAIR* detectors, such as *HADES*, *PANDA*, and *CBM*. To achieve the best time precision, however, each TDC channel must be calibrated individually.

First of all, fine counter calibration should be done by means of random test inputs and it should be repeated, if the calibration function changes (in most cases due to temperature change). Alternatively, temperature dependency of each channel can be calculated in advance and compensated using the temperature information from the sensors around the FPGAs. Another compensation should be applied to the mean value deterioration caused by the temperature change. And finally, stretcher latency (used for ToT measurements), which also depends on the temperature change, should be measured in advanced and compensated during the measurement.

All these calibration tasks can be carried out already during data taking within the event building DAQ software *DABC*. Produced time values can either be stored with the original raw data or replace them. The calibration analysis code has been implemented with the C++ *stream* framework and can run as plug-in for *DABC* as well as with *ROOT*-based analysis environments, like *HYDRA* or *Go4*.

An HTTP server in the *DABC* process provides online monitoring and control of the TDC calibration from a standard web browser.

[1] C. Ugur, S. Linev, J. Michel, T. Schweitzer, M. Traxler, *A novel approach for pulse width measurements with a high precision (8 ps RMS) TDC in an FPGA*, 2016 JINST 11 C01046

Author: LINEV, Sergey (GSI DARMSTADT)

Co-authors: UGUR, Cahit (GSI - Helmholtzzentrum fur Schwerionenforschung GmbH (DE)); ADAMCZEWSKI--MUSCH, Joern (GSI)

Presenter: ADAMCZEWSKI-MUSCH, Joern (GSI)

Session Classification: Poster session 1

Track Classification: Real Time System Architectures and Intelligent Signal Processing