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The TRB3 collaboration
http://trb.gsi.de

Online calibration of the TRB3 FPGA TDC with DABC software

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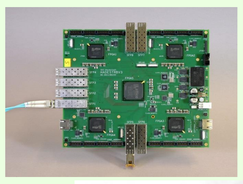
Abstract

The TRB3 - Trigger Readout Board - features 4 FPGA based TDCs with a total of up to 264 channels and a time precision of 8 ps RMS **[1]**. It was applied for various beam tests and is going to serve as a standard DAQ hardware for FAIR detectors, such as HADES, PANDA, and CBM. To achieve the best time precision, however, each TDC channel must be calibrated individually.
First of all, fine counter calibration should be done by means of random test inputs and it should be repeated, if the calibration function changes (in most cases due to temperature change). Alternatively, temperature dependency of each channel can be calculated in advance and compensated using the temperature information from the sensors around the FPGAs. Another compensation should be applied to the mean value deterioration caused by the temperature change. And finally, stretcher latency (used for ToT measurements), which also depends on the temperature change, should be measured in advanced and compensated during the measurement.
All these calibration tasks can be carried out already during data taking within the event building DAQ software DABC. Produced time values can either be stored with the original raw data or replace them. The calibration analysis code has been implemented with the C++ stream framework and can run as plug-in for DABC as well as with ROOT-based analysis environments, like HYDRA or Go4.
An HTTP server in the DABC process provides online monitoring and control of the TDC calibration from a standard web browser.

[1] C. Ugur, S. Linev, J. Michel, T. Schweitzer, M. Traxler, *A novel approach for pulse width measurements with a high precision (8 ps RMS) TDC in an FPGA*,2016 JINST 11 C01046

TRB3 hardware



Photos by G.Otto, GSI

- Main board with 5 Lattice ECP3-150EA FPGAs
- 4 peripheral FPGAs as TDCs with up to 260 channels
- central FPGA for trigger system and GbE controller
- TrbNet (control) and UDP/IP/GbE (data) protocols
- 8 SFP connectors
- 4 highspeed 208 pin connectors for various AddOns:
  6 port hubs, NIM/ECL input, ADC, 100mil pins, PADIWA,..
- reduced variant TRBsc exists (1 FPGA each for 19'' crate system)

Timestamp counters

Dump of acquired TRB3 TDC data with DABC *hldprint* utility:

```
*** Event #0xcb1e71ea fullid=0x2001 runid=0x0eb0eb32 size 536 ***
    *** Subevent size    504 decoding 0x020011 id 0xc940 trig 0x7bb1e7e7 swapped align 4 ***
        *** Subsubevent size  48 id 0x0940 full 00300940
                [  1] 21e70000  tdc header
                [  2] 63089e85  epoch 50896517 tm 5784258560.000 ns
                [  3] 80116af8  hit  ch: 0 isrising:1 tc:0x2f8 tf:0x116 tm:5784262357.315 ns
                [  4] 63089e85  epoch 50896517 tm 5784258560.000 ns
                [  5] 8051aae9  hit  ch: 1 isrising:1 tc:0x2e9 tf:0x11a tm:-75.043 ns
                [  6] 805492f4  hit  ch: 1 isrising:0 tc:0x2f4 tf:0x149 tm:-20.554 ns tot:54.489 ns
                [  7] 63089e85  epoch 50896517 tm 5784258560.000 ns
                [  8] 808e2ae9  hit  ch: 2 isrising:1 tc:0x2e9 tf:0x0e2 tm:-74.435 ns
                [  9] 809372f3  hit  ch: 2 isrising:0 tc:0x2f3 tf:0x137 tm:-25.359 ns tot:49.076 ns
                                ...
```

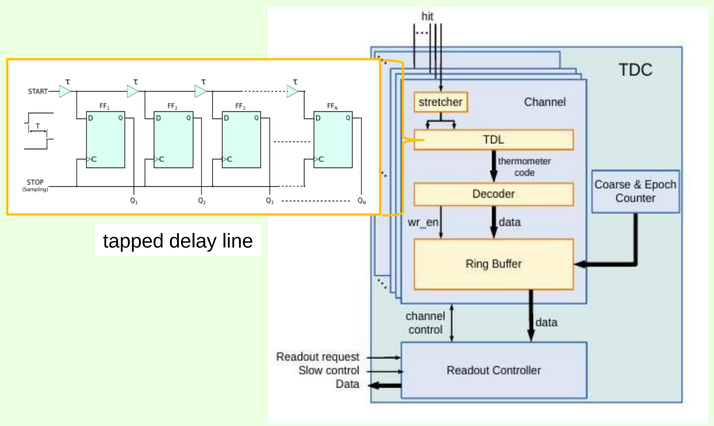
The **hit time** *t_stamp* is evaluated from *epoch* marker, coarse counter *t_coarse* and calibrated fine counter *t_fine*, as denoted by different colors:

$$t\_stamp = (epoch * 2048 + t\_coarse) * 5ns - Calibr(t\_fine)$$

The **Time over Threshold** *T_o_T* is derived from consecutive hits with "rising edge" and "falling edge" properties ("isrising" 1 or 0):

$$T\_o\_T = t\_stamp_{falling} - t\_stamp_{rising}$$

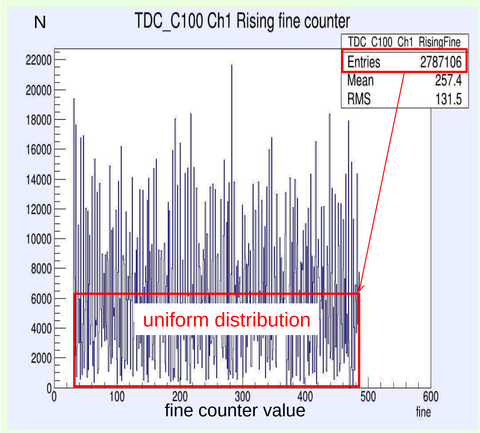
FPGA TDC



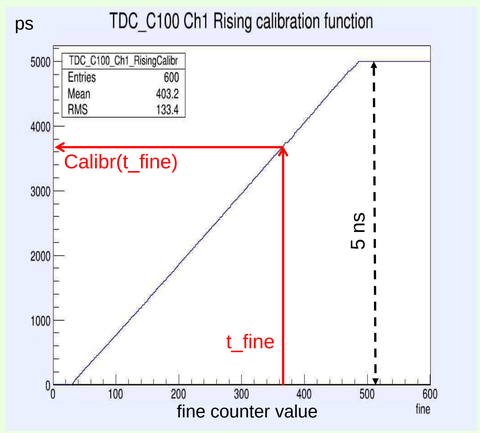
tapped delay line

TRB3 FPGA TDC uses tapped delay line (TDL) technique: Fine time stamp of an incoming signal is derived from the number of delay elements which the signal propagates from arrival until the next 200 MHz readout clock edge stops such sampling. For time over threshold (ToT) measurements, trailing edge is shifted by a stretcher to subsequent readout clock cycles (from **[1]**).

Statistical calibration approach



accumulated fine time counter distribution of a single TDC channel



Resulting calibration function *Calibr(t_fine)*

Assuming input signals with an uniformly fine time distribution, the TDC fine time counter values should also be uniformly distributed in the ideal case. The measured deviations from such uniform distribution can be used to evaluate a fine time counter calibration *Calibr(t_fine)*. Practically this can be implemented as lookup-table or as parametrized function. This calibration requires, however, a sufficient statistics of acquired time values ("hits") for each TDC channel. The calibration procedure may be performed with special triggered signals either once before the actual detector data taking, or it may be repeated frequently, e.g. during accelerator spill pauses.

Online software

Data acquisition for TRB has been implemented with DABC framework (http://dabc.gsi.de). UDP packets, retrieved from several TRB boards, are verified, sorted and combined together into HLD formatted events, which are then stored on disk.
The code for FPGA TDC calibration and temperature compensation has been implemented with C++ based stream framework (https://github.com/linev/stream). This code can be embedded into various higher level frameworks, like ROOT, Go4, DABC or HYDRA.
DABC allows to run TDC calibration code directly in the DAQ process, providing ready-to-use data for further analysis. This simplifies the task of building heterogeneous setups, where different kinds of TRBs boards (with and without FPGA TDC) can be used. The same code can be run also offline, using HLD files as inputs. All stages can be monitored with Go4 GUI or with a web-based UI.

DABC web interface

The complete DAQ process, including data taking, TDC calibration and files storage, can be monitored and controlled by a web interface. One can also access various histograms produced in the TDC calibration process. This web UI has been implemented using the JavaScript ROOT library (https://root.cern.ch/js/).

Temperature dependency

Temperature significantly affects the FPGA TDC fine-counter calibration function. A difference of several degrees K leads to increase of timing errors in 20-40 ps, which is much higher than obtained 8÷12 ps resolution of a TDC with constant temperature. To avoid such effects, temperature should be stabilized or calibration should be repeated constantly, taking into account any possible changes.

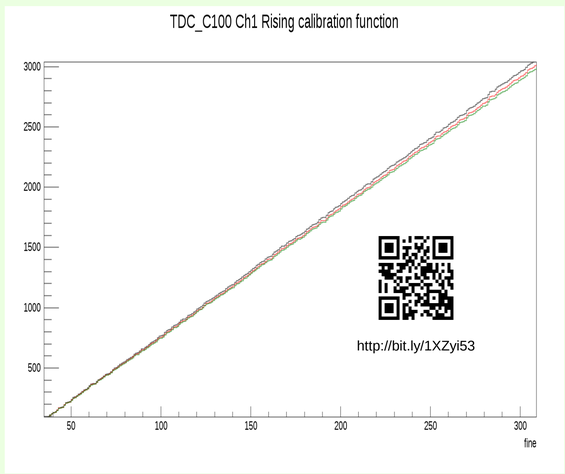
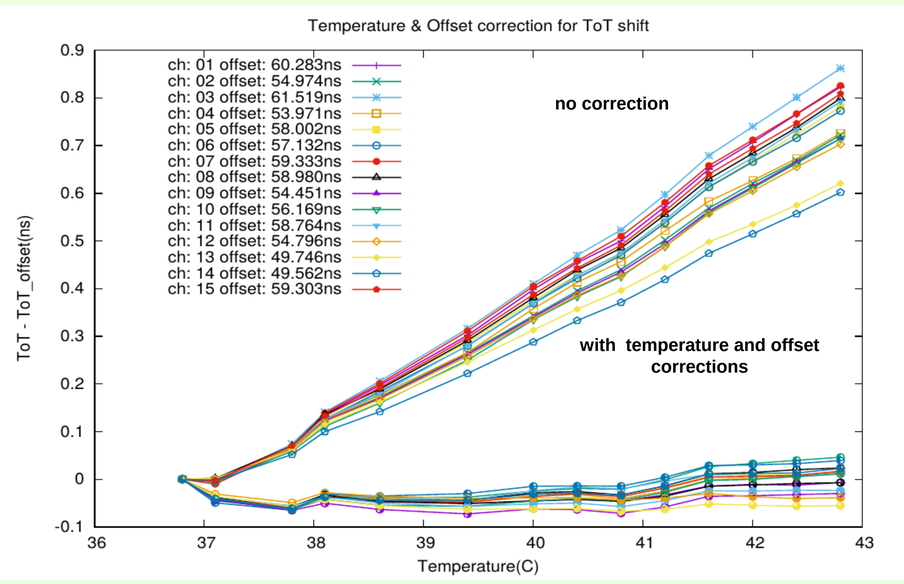


Figure shows the calibration function for the same channel, measured with temperatures **28**, **35** and **44** °C. These calibrations look very similar except for a scaling factor. This can be described by a linear function:

$$Calibr_t(fine) = Calibr_{t0}(fine) \times (1 + 0.0044 \times (t - t0))$$

The described correction compensates most temperature effects on fine-counter calibration. Since a temperature sensor near each FPGA TDC is continuously read out, such correction can be applied online during data taking. The resulting **precision of time measurement in ±5 °C temperature range remains below 18 ps**.

ToT temperature corrections



Time over Threshold (TOT) values measured with the FPGA TDC are also affected by temperature. Both the fine time counter calibration and the stretcher offset for the trailing edge signal are temperature dependent. This deterioration of ~100 ps/ °C can be compensated by individual channel calibration with a pulser signal of known TOT. Such correction can be applied in stream/DABC software already during data taking, since the actual temperature data is also read out from the FPGA. Taken from **[1]**

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