The study of strip Readout Prototype for ATLAS Phase-I muon Trigger upgrade

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***Abstract*–we will present the strip readout prototype for ATLAS small-strip Thin Gap Chamber(sTGC) Phase-I Muon trigger upgrade, which named strip Front End Board(sFEB). The prototype includes 8 VMM2 ASICs for strip signal conditioning, a Xilinx Kintex-7 FPGA for VMM2 configuration and events readout, a commercial ethernet chip working at the physical layer. The sFEB prototype is described in details.**

I. Introduction

ATLAS[1,2] is one of the four experiments at Large Hadron Collider (LHC).LHC will be upgraded in the next several years aiming to new physics study. ATLAS experiment will fulfill Phase-I upgrade by 2018. The current ATLAS muon end-cap system (Small Wheel, SW) [3] will be replaced with the New Small Wheel (NSW). The NSW is a set of precision tracking and trigger detectors able to work at high rates with excellent real-time spatial and time resolution. The small-strip Thin Gap Chamber (sTGC) will devote to trigger function in NSW.

STGC contains pad, wire and strip readout. The pads are used through a 3-out-of-4 coincidence to identify muon tracks roughly pointing to the interaction point (IP). They are also used to define which strips need to be readout to obtain a precise measurement in the bending coordinate for the event selection.

This paper presents the study of sTGC strip Readout Prototype, and it is named strip Front End Board (sFEB). It will accept the pad trigger, which is the external trigger from the trigger unit through a Mini-SAS connector, to define the regions-of-interest for strips readout. Strip signals are received by a VMM2[4,5] ASIC which can handle the signals with the capacity of 64 inputs, and output the trigger data and raw data of hit events. The VMM2 trigger data will be transmitted to a Trigger Data Serializer (TDS) ASIC which is still under development. The raw data will be sent to Read-Out Controller (ROC) ASIC which is also not ready yet. The TDS and ROC functions will be accomplished in FPGA. The sFEB prototype includes 8 VMM2s, a Xilinx Kintex-7 FPGA, and a physical layer Gigabit Ethernet Transceiver(GET). The Graphical User Interface(GUI) is designed with Qt platform

Manuscript received May 30, 2016. This work was supported by the National Natural Science Foundation of China under Grants 11461141010 and 11375179, and in part by "the Fundamental Research Funds for the Central Universities" under grant No. WK2360000005.

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II. Prototype Architecture

A. Hardware

The schematic block diagram of the sFEB prototype is shown in Fig. 1. The core of sFEB is based on a Kintex-7 FPGA, which is configured by a Serial Peripheral Interface (SPI) flash. The FPGA also accomplish the functions of TDS and ROC ASICs, the configuration and data readout of up to eight VMM2s, and all the data transceiver with PC through a commercial Ethernet chip. Eight VMM2s, which are interconnected using a daisy chain, are used to read out the strip signals from the sTGC detector. The overall sFEB has the ability to handle up to 512 channel strip signals. The prototype also enables us to test and understand VMM2, which can help optimize the design of sFEB for the next version.

In the final version of sFEB, there will need four Mini-SAS connectors, one for Pad trigger(IN), one for ROUTER(OUT), and two for Level-1 Data Driver Card(OUT). But on the prototype of sFEB, an ethernet connection is needed. The current RJ-45 connector will be replaced with a Mini-SAS connector in the final version. All the Mini-SAS connectors will connect to FPGA general purpose IO pins.

The photo of sFEB prototype is shown in Fig. 2.

B. Initialization and Data Readout of sFEB

The VMM2 chips need to be configured, the configuration stream is 1616-bit length in one VMM2. All the 8 VMM2s are inter-connected in a daisy-chain, the total configuration stream will be 1616*8bits length. The configuration bit is set in a graphical user interface (GUI). The GUI is designed with Qt platform. The GUI running on a PC will download the command and configuration data to the FPGA through the Ethernet chip. FPGA will decode the command, then works in corresponding modes. All the data from VMM2s will be packaged and transmitted to PC through Ethernet.

The GUI will also decode the event raw data and give out the hit channel number, the BCID, the amplitude and the hit time information of the event.

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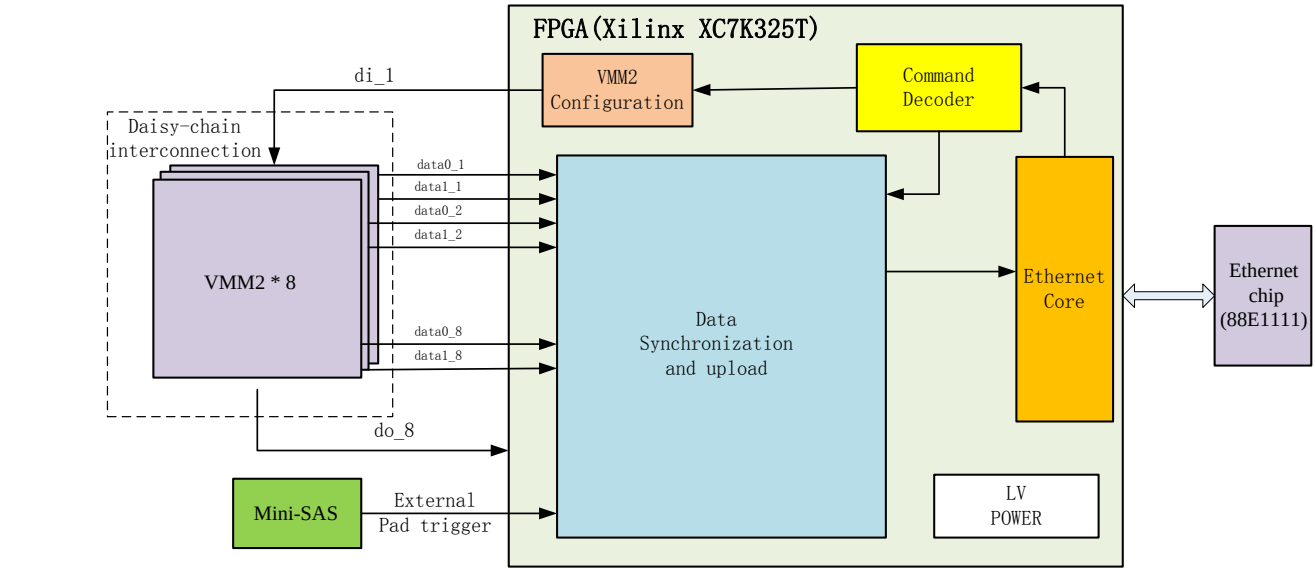

Fig. 1 Block diagram of the strip Readout Prototype (sFEB)

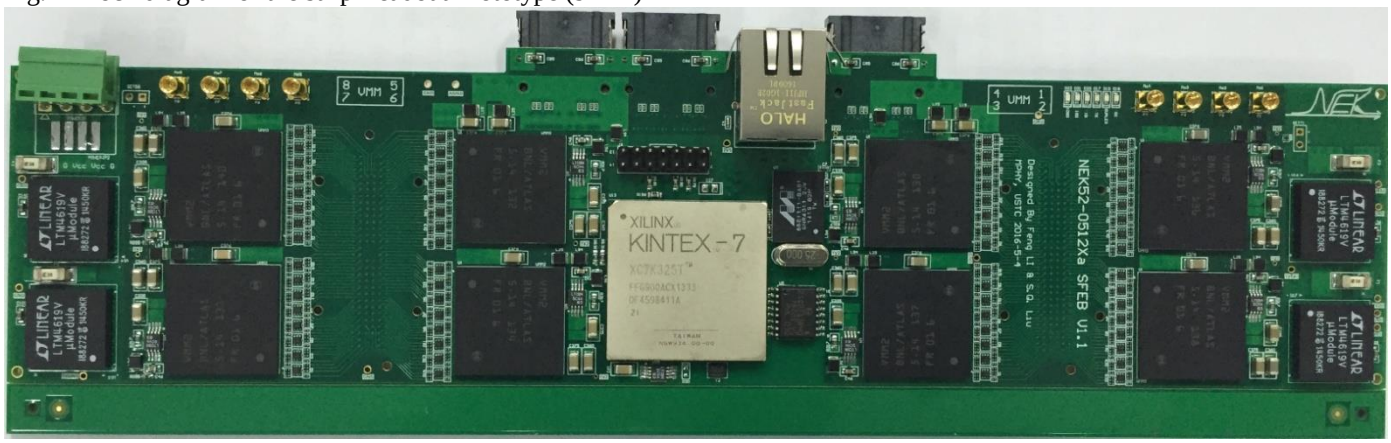

Fig. 2 the photo of sFEB(top view, Mini-SAS connectors are on the bottom layer, the RJ-45 connector will be replaced with another Mini-SAS in the final version)

III. Test Results

The Qt-based GUI will collect the hit event raw data and decode them. Then display the corresponding information. Fig. 3 shows the channel and amplitude test results for all the eight VMM2s. It shows that all the eight VMM2s can work properly.

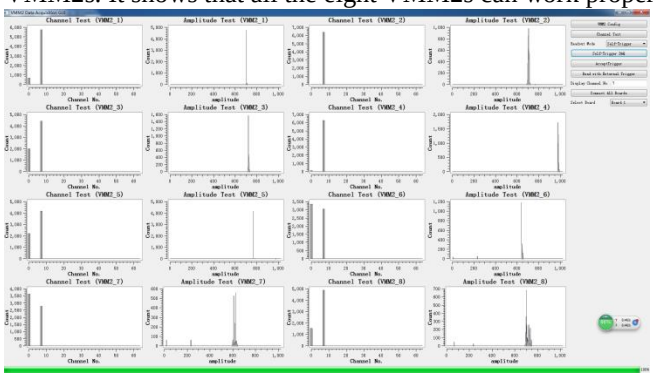

Fig. 3 The eight VMM2

We also can observe the raw data of eight VMM2s through Chipscope of Xilinx FPGA Development Environment(ISE), Fig. 4 shows the readout data recorded in Chipscope.

Fig. 4 VMM2s raw data observed through Chipscope

IV. Conclusion

In this paper, a strip readout prototype based on high performance FPGA and Gigabit Ethernet interface is described. The hardware design and data readout are discussed in details. The sFEB prototype will be used for sTGC chamber performance site test.

Acknowledgment

We want to thank Brookhaven National Laboratory for the VMM2 supply. VMM2 is the key component for our sFEB design.

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