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Design and Testing of the Bunch-by-Bunch Beam Transverse Feedback Electronics for SSRF

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Shanghai Synchrotron Radiation Facility (SSRF) is one of the third-generation high-beam current (3.5GeV) synchrotron light sources. In the storage ring of SSRF, multi-bunch instabilities would increase beam emittance and energy spread, which degrade beam quality and even cause beam loss. To address the above issues, a Transverse Feedback System is indispensable for SSRF, in which the key component is the bunch-by-bunch transverse feedback electronics.

The whole feedback system consists of five main parts: BPM, RF front-end, signal processor, RF amplifier, and vertical/horizontal transverse kickers. This paper focuses on the signal processor, which is the main part of the feedback electronics.

The RF front-end imports the signals from the BPM, then filters them to a bandwidth below 250 MHz, and send them to the signal processor. Then we use a 12 bit 500 Msps ADC (Analogue to Digital Converter) to sample the signal, and the digitized data are transferred to an FPGA (Field Programmable Gate Array) for Digital Signal Processing (DSP). The input data are first deserialized to four 125 Msps data streams, and then the information of each bunch is extracted from the data stream using shift registers, which is then processed by FIR filters to obtain the feedback coefficient of each beam. This coefficient can also be adjusted with different gains which can be controlled via remote PC. To make sure that the kicker takes effect on the correct bunch, the algorithm also contains the delay function with a step size of 4 ns, combined with the external delay line chips, a fine delay step size of 10 ps and a range of 2 μs can be achieved. The output of the FPGA are then converted to analog voltages by 500 Msps DAC (Digital to Analogue Converter). These voltages are then amplified and used as the input of the kickers to tune the beam into the optimum orbit.

We also conducted initial testing on the signal processor to evaluate its performance and function. The test results indicate that the ENOB of the Analog-to-Digital conversion circuits is better than 9.5 bit in the frequency range up to 300 MHz, which is good enough for the application. Besides, this system also functions well as expected.

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