Implementation of ITER Fast Plant Interlock System Using FPGAs with cRIO

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***Abstract*–Interlocks are the instrumented functions of ITER that protect the machine against failures of the plant system components or incorrect machine operation. Regarding I&C, the Interlock Control System (ICS) ensures that no failure of the conventional ITER controls can lead to a serious damage of the machine integrity or availability. The ICS is in charge of the supervision and control of all the ITER components involved in the instrumented protection of the Tokamak and its auxiliary systems. It is constituted by the Central Interlock System (CIS), the different Plant Interlock Systems (PIS) and its networks. The ICS does not include the sensors and actuators of the plant systems but it is in charge of their control. The ITER interlock system shall be designed, built and operated according to the highest quality standards. The international standard IEC-61508 has been chosen as the reference. In both CIS and PIS cases two main architectures are used: a slow architecture, for those functions with response time requirements slower than 100ms (300 ms for central interlock functions), based on PLC technologies, and a fast architecture, based on FPGA technologies, for the functions with faster requirement times. The proposed design for fast PIS is based on the use of RIO (Reconfigurable Input/Output) technology from National Instruments (compactRIO platform). In order to provide a high integrity solution, a FMEDA (Failure Modes Effects and Diagnostics Analysis) has been conducted to analyze the components behavior. According to the output of the FMEDA a set of diagnostics has been defined and additional redundancy was added to the architecture to improve the integrity figures. The defined configuration has been called the "double-decker solution", with two chassis running in parallel, communicated between them using a synchronous high speed serial line, and using redundant modules to implement the input and output measurement/excitations and redundant analog and digital modules to implement the diagnostics of these input/output modules. The integrity figures for the "double decker" solution are obtained from the classification of the failure rates, obtaining for the different configurations a SFF (safe failure fraction) of 85% and a FPH (Probability of dangerous Failure per Hour) of less than 1E-07. The FPGA design includes all the hardware to support the data acquisition from the input modules, the implementation of the diagnostics functionalities for analog and digital modules, the voting schema and the activation/deactivation of digital outputs. The platform includes an external test platform, also based on compactRIO technology, to perform the validation of the system and to register the performance of the different interlock functions implemented. The response times obtained for the TTL input to TTL output interlock function ranges from 5µs to 20µs; for the analog input to TTL output the response time is in the range of 41 µs to 90 µs, and for interlock functions using 24V digital input to 24V digital output, the time can rise up to 643 µs.**

I. System Description

Interlocks are the functions in charge of protecting ITER machine against failures of the different plant system components or incorrect machine operation. The ITER Interlock Control System (ICS) is constituted by the Central Interlock System (CIS), the different Plant Interlock Systems (PIS) and its networks [1]. The ICS does not include the sensors and actuators of the plant systems but it is in charge of their control. The CIS is in charge of implementing the Central Protection Functions in ITER using the different PIS with the help of specific networks or direct hardwired actuators. It also provides access to the local interlock data of the different Plant Interlock Systems (Fig.1). ITER ICS has been designed to obtain different levels of integrity that have been defined as 3IL-2 to 3IL-3 according to the value of PFD (Probability of Failure on Demand) and PFH (Probability of dangerous Failure per Hour) equivalent to the SIL (Signal Integrity Level) values defined in the IEC 61508 [2]. Central Interlock system and plant interlock system include fast and slow controllers to implement the specific interlock functions. The slow controllers are implemented with PLC and the fast ones with FPGA-based solutions using NI cRIO systems [3]. From the technological point of view, the design of a fast controller that meets the requirements of 3IL-3 is an important challenge.

In order to meet this requirement the solution proposed for Fast Interlock System uses two cRIO systems in a double decker architecture with redundancy and diagnostics. Both cRIO chassis (every cRIO chassis has an XILINX FPGA) are interconnected between them using a communication link used to interchange the status. The implementation done covers different setups in order to implement analog and digital interlock functions using 24V and TTL signals.

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Fig. 2 shows an example with analog inputs with a 2oo3 voter schema and 24V digital outputs [4].

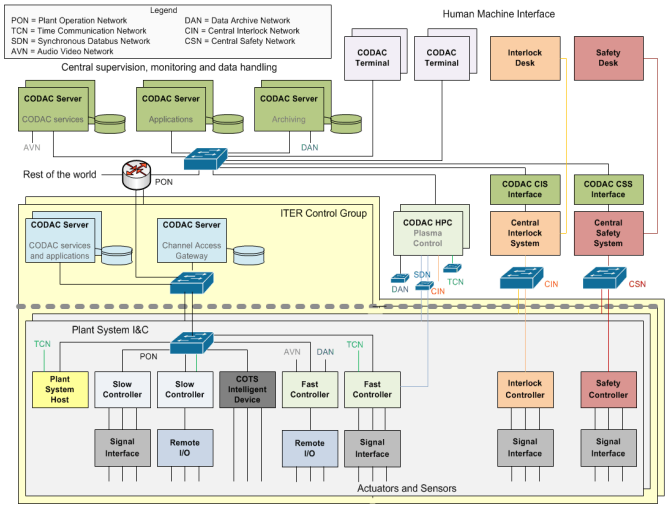

Fig. 1. Plant Interlock Systems

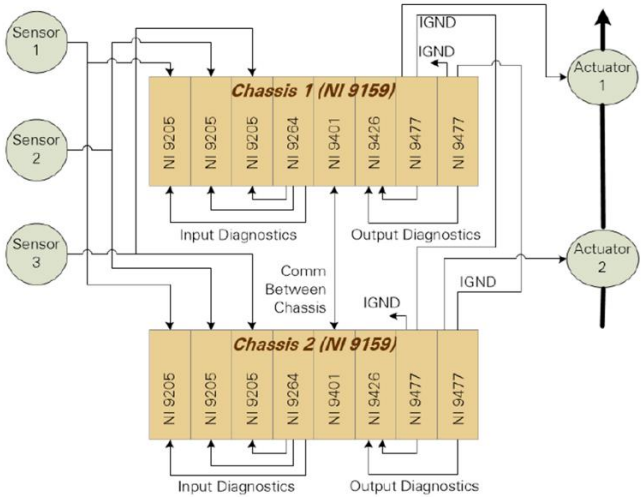

Fig. 2. System example with analog inputs with a 2oo3 voter schema and 24V digital outputs

In all different configuration the logic implemented in the FPGA is very similar and it is represented in Fig. 3. The FPGA takes the data from the input modules and implements the diagnostic of these modules (this also requires that the FPGA generates the analog or digital patterns for diagnostics), the results are passed through a voter, which is also verified internally, and the outputs are generated after the corresponding verification of the output modules, if all the diagnostics and results are correct. These logic processes have been parallelized in order to reduce the response time of the solution.

Table 1 summarizes the values obtained for the three developed configurations indicating: the value of PFH, the value of this PFH in % with respect to the limit stablished in IEC-61508 for a SIL3 system, the value of SFF and range obtained for the response time.

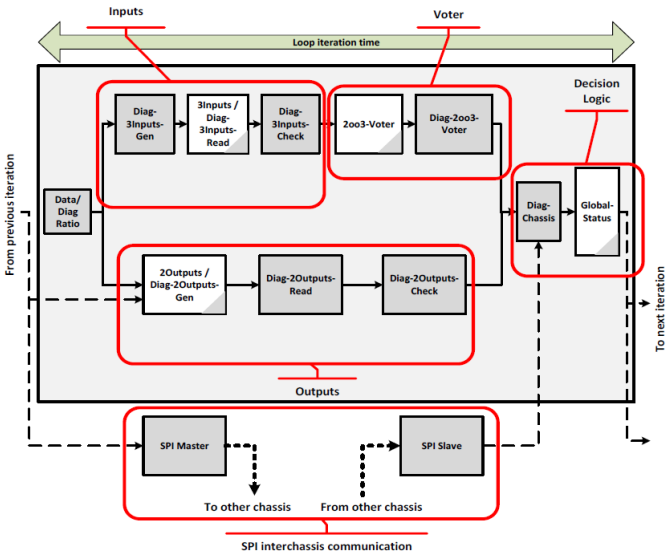

Fig. 3. Block diagram of the logic implemented in the FPGA

TABLE I. RESULTS

Conf.	Description	PFH	% of SIL3. (IEC 61508)	SFF	Response Time range
A	3 Analog Inputs – 2 Digital Outputs 24V	1.324 E-8	13.2%	85.47 %	[41-89] µs
B	3 Digital Inputs 24V – 2 Digital Outputs 24V	1.322 E-8	13.2%	85.47 %	[143-643]µs
C	3 Digital Inputs TTL – 2 Digital Outputs TTL	1.597 E-8	16%	85.47 %	[5-20] µs

REFERENCES

[1] Antonio Vergara et al. "Modeling tools for the ITER Central Interlock System" Fusion Engineering and Design 86 (2011) 1137–1140.

[2] IEC 61508: Functional Safety of electrical/electronic/programmable electronic safety-related systems.

[3] http://www.ni.com/compactrio

[4] Birolini, Alessandro; "Reliability Engineering - Theory and Practice;" Fourth Edition, 2004; Springer.

[5] Sin-iti Kitazawa, Katsumi Okayama, Yuzuru Neyatani, Francois Sagot, Didier van Houtte, RAMI analysis of the ITER CIS, Fusion Engineering and Design, Volume 89, Issue 2, February 2014, Pages 88-93, ISSN 0920-3796, http://dx.doi.org/10.1016/j.fusengdes.2013.12.016. (http://www.sciencedirect.com/science/article/pii/S0920379613007308).

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