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PLAS: A 32-channel, dead time-less analog memory ASIC fpr the TRACE detector

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TRACE is a new detector based on silicon pad technology for detection of particles and light ions in fusion evaporation and direct nuclear reactions, whose identification relies on pulse shape analysis and requires sampling pulse windows of 1 us at 200 MHz with strong restrictions on power, area and connectivity. Local triggering, pulse sampling, zero suppression and serialization thus have to be carried out at the front-end.

An analog memory ASIC named PLAS (for PipeLined Asymmetric SCA) has been designed for these tasks. The circuit contains 32 independent input channels whose polarity, bias point and gain can be selected with an external resistor and programmable parameters such as reference voltage, comparator thresholds and local trigger conditions, which may be configured through an I2C interface.

A novel analog memory architecture is presented that splits the typical Switched Capacitor Array (SCA) in two asymmetric stages connected with a switching matrix. The first stage has a 32-cell SCA per input that is continually sampling. The second one has 8 shared slots, each with a 192-cell SCA for pulse sampling and a 32-cell SCA that acts as a storage buffer. When an input is triggered, a free slot in the second stage is assigned where post-trigger samples are acquired by the 192-cell SCA. Meanwhile, the 32 pre-trigger samples are transferred to the 32-cell storage buffer in the second stage. As capture ends, the contents of the first stage have been copied and sampling resumes immediately with no dead time.

SCA stages capture samples using both edges of a 100 MHz clock. A dedicated interface is used to read out stored data serially at 50 MHz in a frame format containing the analog samples and digital data such as the trigger timestamp. The second stage is managed like a FIFO queue.

The advantages of this architecture are the lack of readout-related dead time, which is a novel feature, and area reduction by sharing storage resources between many inputs and expecting relatively low rates and multiplicities. The downsides are increased calibration complexity, different response for pre- and post-trigger samples, and fixed pre-trigger window sizes.

The ASIC has been implemented in 0.18 um CMOS technology with 1.8 V supply and has a die size of 3.5 mm x 3.9 mm. Simulated performance predicts around 100 MHz bandwidth, 12 ENOB and 10 mW per channel. The circuit was sent to foundry in November 2015; samples are expected in February 2016 and the first test results should be available by June 2016.

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