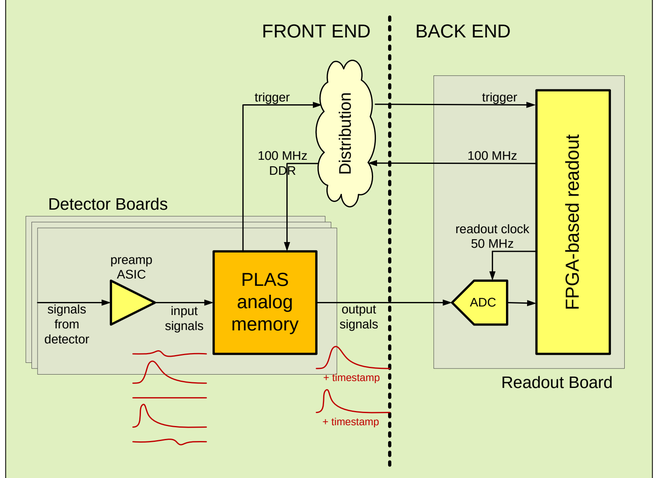
PLAS: A 32-CHANNEL, DEAD TIME-LESS ANALOG MEMORY ASIC FOR THE TRACE DETECTOR

R. J. Aliaga[1*], V. Herrero[2], S. Capra[3], J. A. Dueñas[4], A. Pullia[3], A. Gadea[1], D. Mengoni[5]

[*]**Contact:** ***raalva@ific.uv.es***

PURPOSE

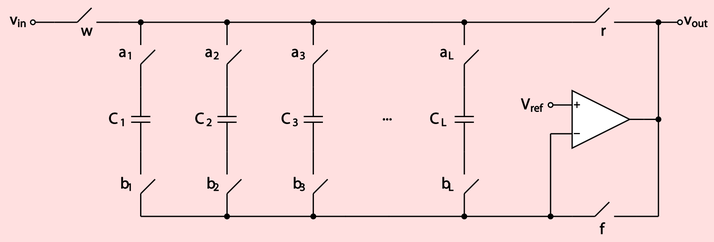


PLAS is a low power, compact ASIC for the TRACE front-end that carries out:

- zero suppression
- local triggering
- timestamping
- pulse sampling
- serialization

ANALOG MEMORY ARCHITECTURE

SCA (Switched Capacitor Array)



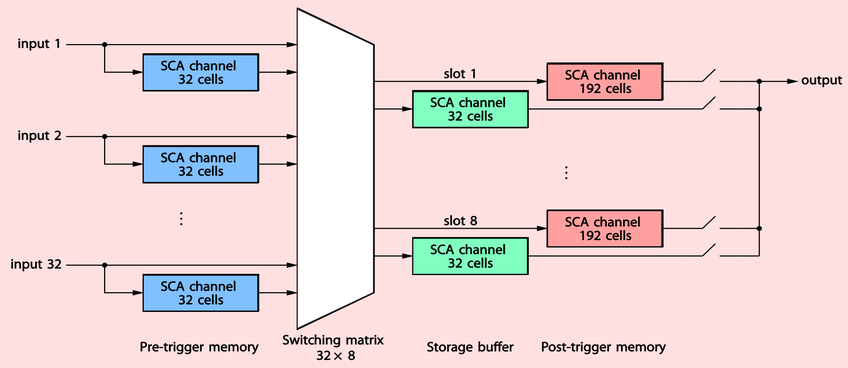
Typical analog memory circuit: one SCA per channel.

- Capacitors sequentially connected to bus to write analog voltage values until stopped by trigger.
- Read out later one by one and digitized externally.
- High write frequency, low read frequency.

Problem: Cannot be rewritten until read out. Limited by read frequency. **Very long dead time.**

Existing solutions: Partial readout, channel replication.

PLAS (PipeLined Asymmetric SCA)



New solution: Split the memory into two sequential SCA stages.

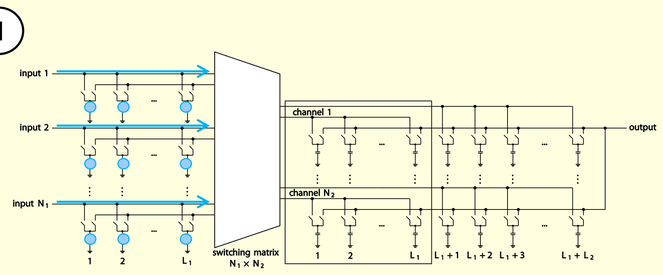
- **Stage 1:** **One short SCA** per channel for pre-trigger samples.
- **Stage 2:** A few slots containing **one long SCA** for post-trigger samples and **one short SCA** to store a copy of Stage 1.

Advantages: *no deadtime, reduced number of cells*

Disadvantages: *more complex calibration, noisier pre-trigger*

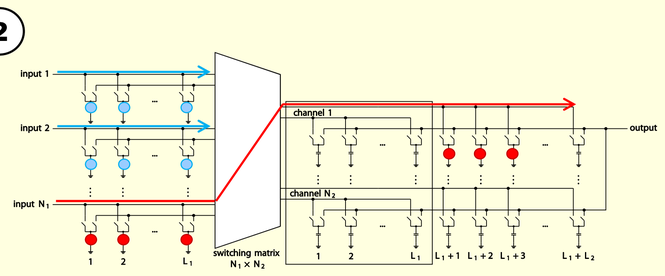
PRINCIPLE OF OPERATION

1



The 1st stage is sampling like a circular buffer.

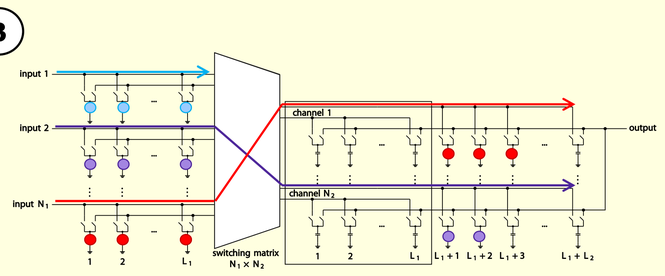
2



On trigger, the channel is locked.

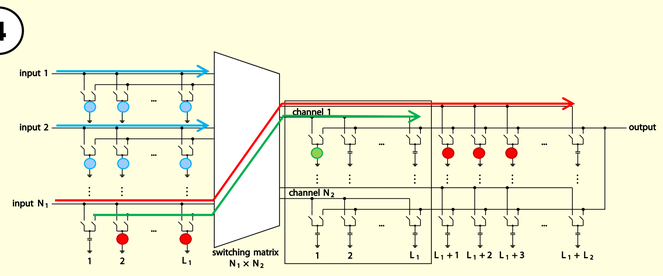
Capture continues at a free slot in the 2nd stage.

3



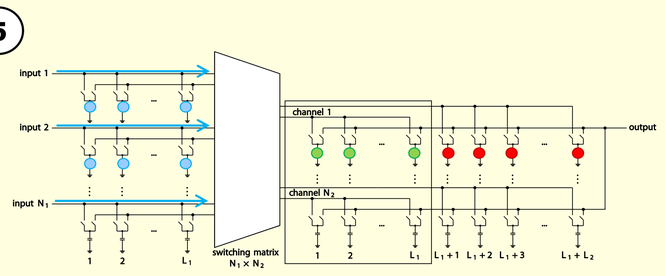
Simultaneous capture of different channels is possible.

4



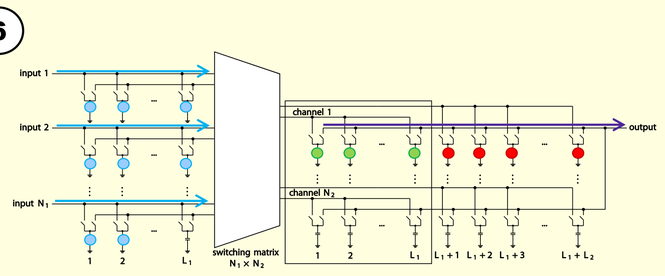
During capture, 1st stage samples are copied to a buffer in the 2nd stage.

5



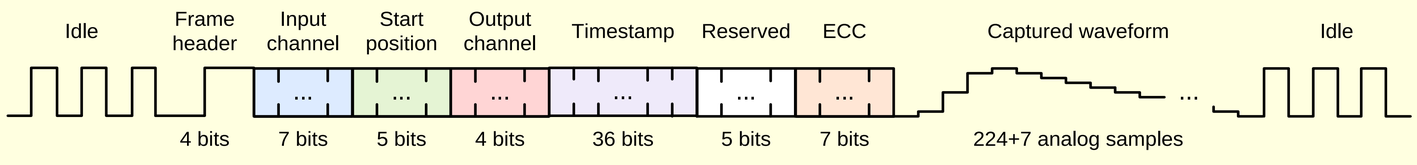
After capture, the 1st stage is ready again.
No deadtime.

6



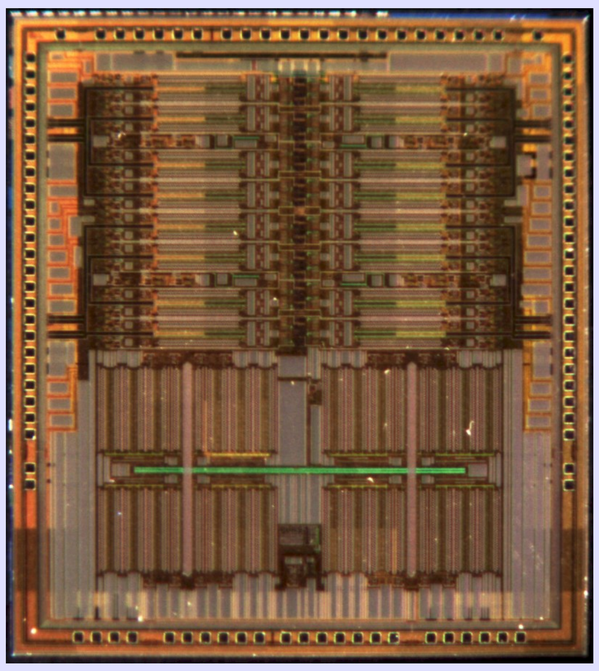
The captured pulse samples are read out later at a slower rate.

7 Readout is organized in frames with analog samples and digital data (timestamp and internal tracking).

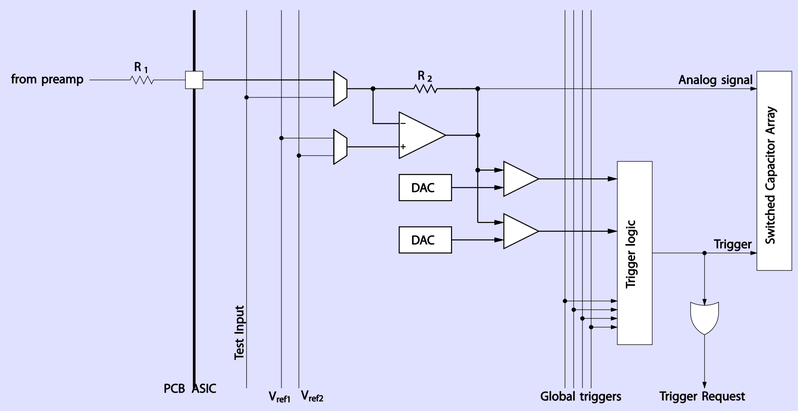


PROTOTYPE

PLAS prototype specifications	
Technology	0.18µm CMOS
Die size	3.5 × 3.9 mm^2
Input channels	32
Queue slots	8
Memory depth	224 per slot (32 pre-trigger + 192 post-trigger)
Write frequency	200 MHz (100 MHz DDR)
Read frequency	50 MHz
Power supply	1.8 V
Internal range	0.3 V to 1.5 V
Simulated performance	
Input bandwidth	100 MHz
Output noise	11.9 ENOB
Power consumption	10 mW/channel



Input channel features	
Input polarity	Configurable
Input range	Configurable (external resistor)
Trigger mode	Programmable
Trigger threshold	Programmable, 2 per channel



Poster presented at the 20th Real Time Conference - June 2016, Padova, Italy.

Partially supported by the Spanish Ministry of Economy and Competitiveness (MINECO) under Grant FPA2014-57196-C5, the Generalitat Valenciana, Spain, under Grant PROMETEOII/2014/019, and the European Comission FEDER funds.

[1] *Instituto de Física Corpuscular (IFIC, CSIC-UV), Valencia, Spain*
[2] *Instituto de Instrumentación para Imagen Molecular (I3M, UPV), Valencia, Spain*
[3] *Istituto Nazionale di Fisica Nucleare (INFN) - Sez. di Milano, Italy*
[4] *Departamento de Física Aplicada, Universidad de Huelva, Spain*
[5] *Istituto Nazionale di Fisica Nucleare (INFN) - Sez. di Padova, Italy*