PLAS: A 32-Channel, Dead Time-less Analog Memory ASIC for the TRACE detector

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***Abstract*—An analog memory ASIC named PLAS (for PipeLined Asymmetric SCA) is presented that is responsible for local triggering, pulse sampling, zero suppression and serialization at the front-end section of the readout electronics for the TRACE silicon pad detector, where strong restrictions on power, area and connectivity are in place. PLAS contains 32 independent input channels with configurable polarity, bias point, gain and trigger conditions, samples windows of 1 µs of incoming signals at 200 MHz using both edges of a 100 MHz clock, and outputs data serially at 50 MHz in a frame format containing both analog samples and digital data such as trigger timestamps. The analog memory is based on a novel architecture wherein the typical Switched Capacitor Array (SCA) structure is split into two stages connected through a switching matrix. The first stage contains one short SCA per input channel that samples continuously, and the second stage contains a small number of longer SCAs that only become active in case of a trigger; sharing storage resources results in reduced area. Dead time is completely removed by copying the contents of the first stage to a storage buffer in the second stage during acquisition. PLAS is implemented in 0.18 µm CMOS technology with a die size of $3.5 \times 3.9\,\mathrm{mm}^2$. Simulations predict around 100 MHz bandwidth and 12 ENOB with a power consumption of 10 mW per channel; test results are not available yet.**

***Index Terms*—Analog memory, ASIC, dead time, detector readout, front-end electronics, Switched Capacitor Array (SCA), triggerless data acquisition, waveform sampling.**

I. Introduction

The TRacking Array for light Charged particle Ejectiles (TRACE) [1], [2] is a new telescope detector system based on double silicon layers, used for the discrimination of particles and light ions in fusion evaporation and direct nuclear reactions and designed to work in combination with a large gamma tracking array like AGATA [3]. Identification of different ions and particles relies on both ΔE-E discrimination and pulse shape analysis (PSA) [4] based on the sampling of all detector pulses generated at the silicon pads. The first experimental tests using temporary readout electronics [5] have established that acquisition windows of 1 µs at 200 MHz sampling frequency or higher are required for PSA [6] as imposed by the fast signals induced by light particles [7].

The final readout system for TRACE requires monitoring a large amount of detector channels and sampling all generated pulses. One front channel per silicon pad is required for particle discrimination, plus one back channel per layer with opposite polarity that will be used mainly for spectroscopy. An event rate in the range of tens of kHz is expected, and an energy resolution below 1 % at 5 MeV is to be obtained at room temperature. The small dimensions of the reaction chamber impose strong restrictions on front-end circuit size, power dissipation, and connectivity: the complete front-end circuitry for each detector needs to fit in a $25 \times 50\,\mathrm{mm}^2$ circuit board and all captured information should be transmitted serially in order to keep cabling to a minimum, with an estimated maximum power budget around 20 mW per channel.

A triggerless readout scheme has been proposed in [8] where sampling, zero-suppression and serialization are performed at the front-end. A custom Switched Capacitor Array (SCA)-based analog memory ASIC named PLAS (for *PipeLined Asymmetric SCA*) has been designed to perform these tasks [9]. The circuit receives detector signals processed by tunable charge preamplifiers [10], detects valid pulses on any channel, samples them using both edges of a 100 MHz clock and stores the results together with their associated timestamps, which are later read out through a single analog output at 50 MHz and digitized remotely. The ASIC is based on a novel analog memory architecture with the specific purpose of minimizing detector dead time and area occupation per channel. The final version is intended to host 64 or 128 input channels; a first prototype with 32 input channels is described in this text instead.

II. PLAS Architecture

The principle of operation of the analog memory ASIC is based on sequential stages of SCAs. These circuits are frequently used as low-power substitutes for flash ADCs and allow fast analog sampling of transient signals that are stored as charge in internal capacitors and can be later read out at a slower pace. Some of the most representative examples are described in [11]–[14].

Fig. 1 depicts the circuit used to implement a single SCA channel in PLAS, featuring a common operational amplifier that assists in writing and reading operations. The input signal

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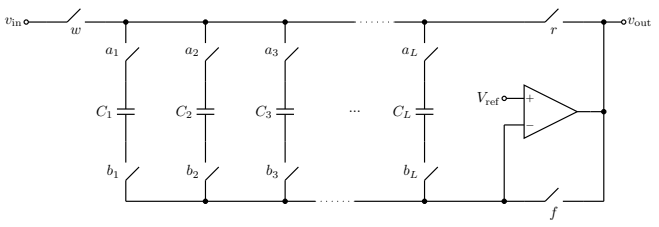

Fig. 1. Implementation of a single SCA channel using a common operational amplifier. Odd and even capacitor switches are controlled by alternating clock edges for double sampling rate; two capacitors are active at any given time.

is connected through a switch w to a common bus from which $L = 32$ storage cells hang, each containing a capacitor and a pair of control switches. With switches w and f closed and r open, cell C_i is written by closing switches a_i and b_i, so that the bottom plate of C_i is biased at a reference voltage $V_{\rm ref}$ while its top plate tracks the input signal. When switches a_i and b_i are opened, the capacitor holds the analog signal value at opening time. Switches in consecutive cells are closed and opened sequentially using both edges of the 100 MHz input clock, so that two cells are activated at any given time, and the channel always holds successive samples corresponding to the last 160 ns of the input signal. When a trigger condition is met for the channel, the continuous writing operation is stopped by opening all switches. A readout process may begin afterwards by closing switch r and then closing switch pairs a_i and b_i sequentially in order to dump the stored voltage values into the bus and to the output with a 50 MHz read frequency. These voltage values are then sampled using an external ADC.

In a typical analog memory device, this SCA structure is merely replicated for each input channel. A problem arises in that the SCA cannot be rewritten until read out, or else the capacitor contents will be overwritten. This causes unwanted dead time in the channel because the read operation is slower than the write operation. Existing solutions usually involve either partial readout [13], [15] or inefficient replication of resources [16], [17].

A different solution is proposed here that relies on splitting the whole memory asymmetrically into two sequential SCA stages connected through a full-mesh switching matrix. The PLAS scheme is shown in Fig. 2, where the circuit has been divided into a first stage that contains a 32-cell SCA channel for every input (*pre-trigger memory*), that is continuously capturing and always contains the last 32 samples, and a second stage with 8 slots meant to actually store the captured signals, each with two SCA channels of sizes 192 and 32 respectively (*post-trigger memory* and *storage buffer*). When an input causes a trigger, the corresponding channel in the first stage is write-locked and its samples are held, a free slot in the second stage is assigned and both are connected through the switching matrix. The timestamp is stored, and signal capture continues at the 192-cell channel. During that time, the contents of the first stage are sequentially read and copied to the 32-cell SCA channel in the second stage, so that the transfer is complete by the time the 192-cell channel is full. At that point, the first stage is immediately ready to start sampling again, so no dead time is introduced. The whole captured pulse remains stored in the second stage slot, consisting of 224 samples corresponding to a 1.12 µs capture window; it can be read out later using a separate interface.

III. ASIC Description

The block diagram of the ASIC prototype is outlined in Fig. 3, with simplified depictions of the input stage and SCA channels. PLAS hosts 32 independent input channels with the structure shown in Fig. 4, each consisting in an inverting voltage amplifier that adapts the preamplifier output range to that of the SCA, between 0.3 V and 1.5 V. Resistor R_1 is external and reference voltages $V_{\rm ref}$ are programmable; proper selection of these two values allow compatibility with different input voltage ranges and polarities in separate channels. Two reference voltages are generated for every group of eight channels using internal DACs. A common test input is also included for calibration purposes.

Trigger modes can be configured individually for each channel. Two comparators with programmable voltage thresholds are included per channel, that allow simple leading edge discrimination using the first one as well as hysteresis by inhibiting further triggers until the second one detects the pulse signal crossing a lower threshold, in order to avoid false triggers due to noise on the falling edge. Four global, external trigger signals are also available, the sensitivity to which can be programmed independently for each channel in order to implement additional functionality. All of these parameters are configured through an I^2C interface.

A dedicated interface is used for the readout of captured events. Readout is timed with the input clock at 50 MHz. Event data are output as analog differential signals through an integrated differential amplifier and a line driver external to the ASIC. Data are digitized by an external ADC at the back-end, and include both analog waveform samples and the digital data encoded as analog values; they must be decoded by the receiving FPGA after digitization.

An training sequence of alternating zeros and ones is output during idle mode, i.e. when no pulse information being transmitted. A 4-bit header indicates the start of a new event frame with the format outlined in Fig. 5. 64 bits of digital data include the timestamp and identification of the queue slot, input channel and cell position where the trigger was issued. These data are enough to completely identify events and their full source and path through the ASIC for calibration correction. In particular, the pulse timestamps must be used to determine whether different pulses belong to the same event, because event reception latency is not deterministic due to the FIFO queue. A 7-bit Hamming error-correcting code (ECC) is computed by the readout controller and included in the frame that allows correction of single bit errors and detection of double bit errors. Finally, the 224 captured samples are transmitted serially, with 7 wait cycles in between due to the internal organization of the SCAs in 32-cell sections. Complete transmission of a single event takes 5.98 µs.

IV. Discussion

The main advantage of the PLAS structure is the area reduction, as the number of total memory cells is reduced

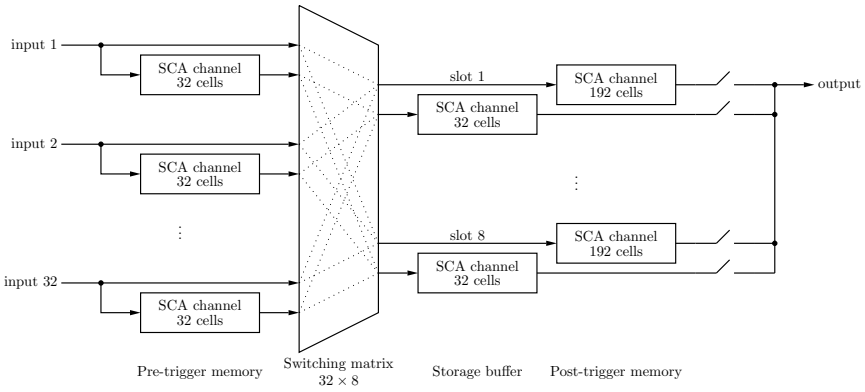

Fig. 2. Pipelined SCA architecture with separate channels for pre-trigger (left) and post-trigger (right) memory connected through a switching matrix. An additional channel in the right section acts as a storage buffer for the pre-trigger memory.

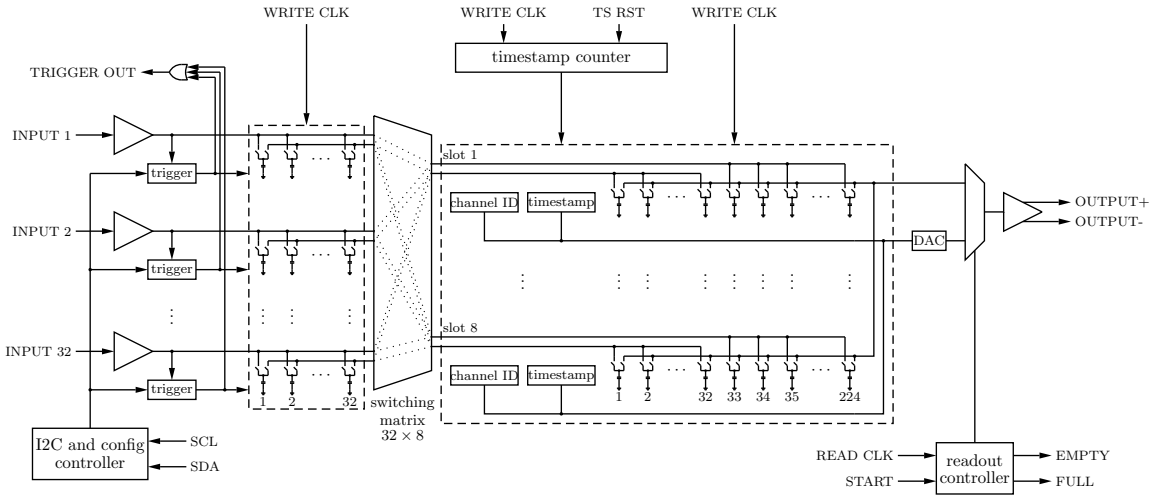

Fig. 3. Simplified block diagram with the main ASIC components and interface signals.

from the $32 \times 224 = 7168$ required in a full SCA structure to $32 \times 32 + 8 \times 224 = 2816$. This is accomplished by sharing storage resources among all input channels; the reduction factor depends on the dimensioning and is better for higher amounts of input channels. Another advantage is the lack of readout-related dead time for single channels, which is a novel feature to the best of the authors' knowledge: the ASIC only exhibits dead time when the output queue is completely full, and all input channels are simultaneously locked in that case. Both advantages exploit the fact that the intended application in the TRACE detector has relatively low event rates and multiplicities.

This architecture also presents some disadvantages compared to the use of full channels for every input. The main drawback comes in the form of different circuit response for pre- and post-trigger samples, as they are processed along separate paths. This increases the complexity of the calibration and correction procedures. Additionally, pre-trigger samples undergo an extra copy operation when being transferred from the first into the second stage, whereby additional noise is introduced. However, pre-trigger samples will be mainly used for estimation of constant baseline levels so the impact of this SNR difference will be largely diminished. One further disadvantage is a slight loss of flexibility, in that the amount of pre-trigger samples is fixed and the maximum number of pulses stored simultaneously is lower.

V. Summary

An analog memory ASIC design has been presented, based on a novel analog memory architecture wherein the typical SCA structure is split into two pipelined, asymmetric stages and captured data are stored in an analog FIFO queue, resulting in reduced area requirements and removing readout-related dead time. The prototype ASIC is intended for the front-end readout of the TRACE detector but generic enough that it can be used with other detectors or applications.

The ASIC has been designed on $0.18\,\mu$m CMOS technology with $1.8\,$V power supply for reduced area and power consumption. The final fabricated prototype is shown in Fig. 6, with a die size of $3.5 \times 3.9\,\text{mm}^2$. Only simulated performance is available at this point, suggesting an input signal bandwidth over $100\,$MHz and noise performance close to 12 ENOB in the worst case (i.e. pre-trigger samples) with power consumption around $10\,$mW per channel.

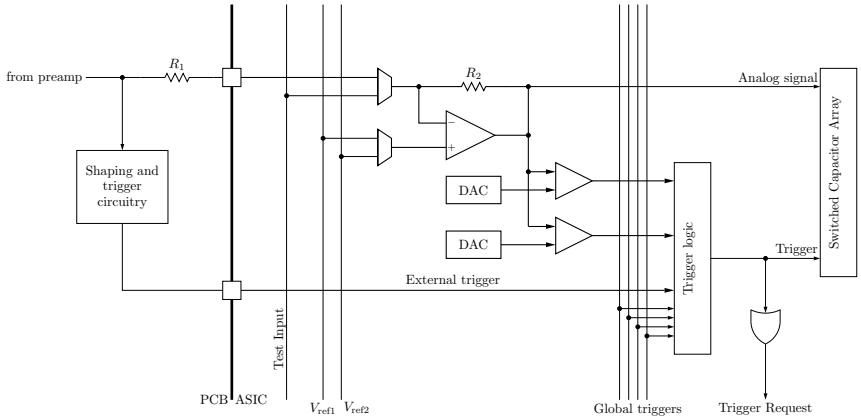

Fig. 4. Diagram of the input stage for each analog memory channel.

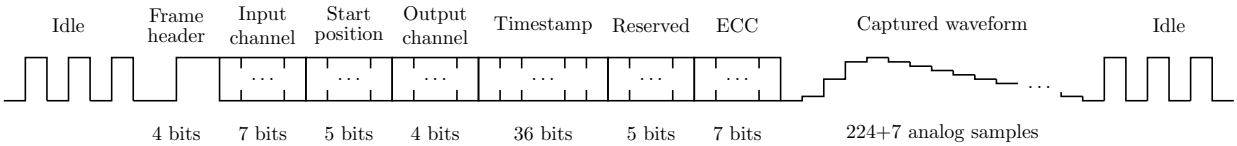

Fig. 5. Event frame format.

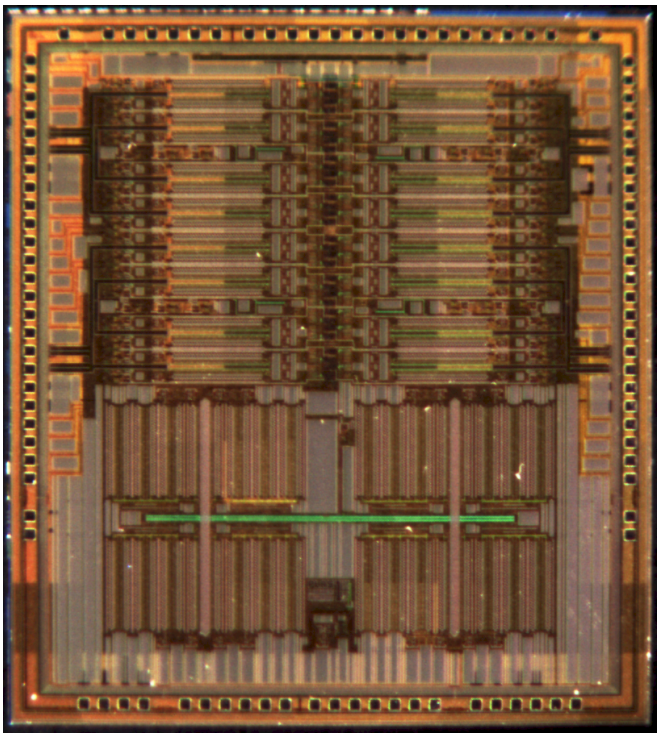

Fig. 6. Photograph of the PLAS die. The first and second SCA stages correspond to the top and bottom halves, respectively. The switching matrix is located in the middle of the first stage.

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