A Time-to-Digital Converter Based on a Digitally Controlled Oscillator

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***Abstract* – Typically, TDAQ systems of High Energy Physics experiments, require time measurements, for example in synchronization or calibration activities. Usually, mixed-signal design is used for the design of time measurement circuits, but in the recent past the research is also studying all-digital design, that have many advantages with respect to the previous approach.**

In this work, we present a full-digital TDC application, based on a synthesizable DCO. The DCO design is technology-independent, it is described by means of a hardware description language and it can be placed and routed with automatic tools.

We present the TDC architecture, the DCO performances and the results on a preliminary prototype, implemented on a 130 nm ASIC.

Index terms— TDC, DCO.

I. Introduction

Typically, TDAQ systems of High Energy Physics experiments, require time measurements, for example in synchronization or calibration activities [1], [2]. Usually, mixed-signal design is used for the design of time measuring circuits, with analog and digital elements working together in the system [3], but in the recent past the research is also studying all-digital designs [4], [5], that have many advantages with respect to the previous approach.

Mixed signal designs can reach better performances, but they require a longer implementation and optimization time with respect to a full-digital design. Furthermore, an analog IP block cannot be easily ported into a new technology, while this can be easily done with digital IPs, in particular when the digital circuit is designed by using a synthesizable hardware description language (HDL), which can be used with automatic Place&Route tools.

In this paper, we present a full-digital TDC application, based on a synthesizable DCO, where the TDC measures the phase relationship between a 40 MHz reference clock and an input signal, with a programmable resolution (obtained by dividing the period of the reference clock in a programmable number of intervals, or steps), as sketched in fig.1.

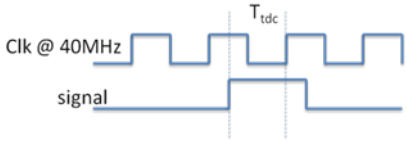

Fig. 1. Phase relationship measured

II. Architectural Implementation

A simplified block scheme of the TDC architecture is shown in fig. 2.

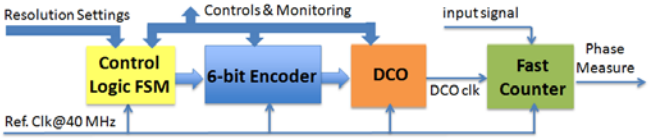

Fig. 2. Simplified block diagram of the TDC.

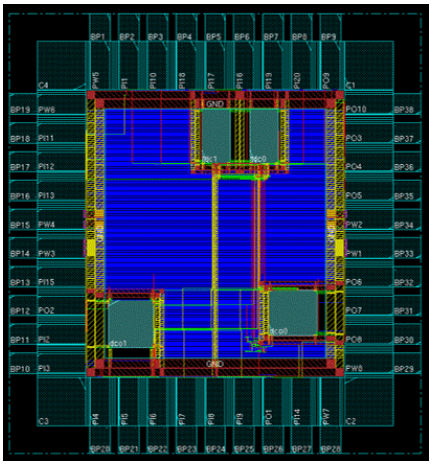

Fig. 3. ADV2 layout picture.

The synthesizable DCO is controlled by a digital logic based on FSM, and an encoder, which sets the DCO output frequency clock, which is then used to drive a fast counter performing the phase measurement between the 40 MHz reference clock and the input signal. During calibration, DCO frequency is adjusted according with the comparison result between the Fast Counter output and the expected value depending on the resolution requested.

In fig. 3 the layout of the first prototype of the chip, which includes two DCOs and two TDCs is shown.

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III. Test Description And Results

In fig. 4 the experimental setup used for the test of the first prototype of the chip is shown.

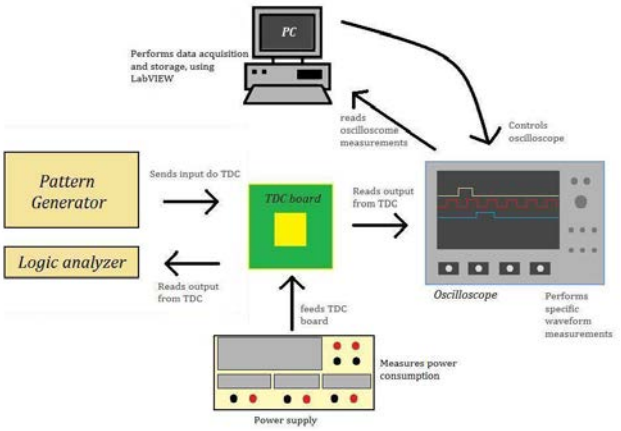

Fig. 4. Scheme of the setup for the ADV2 chip test.

A mixed-signal oscilloscope is used to measure the phase of the test signal w.r.t. the system clock (both taken on probe points on the board) and to register the TDC output. These data are acquired by a PC, where the TDC response is compared with the phase measured with the oscilloscope.

Tests are performed by setting the resolution required, by sending an input signal with a certain phase w.r.t. the 40 MHz master clock and spanning all the phase range.

For each test signal, the phase measured by the scope is compared with the TDC output.

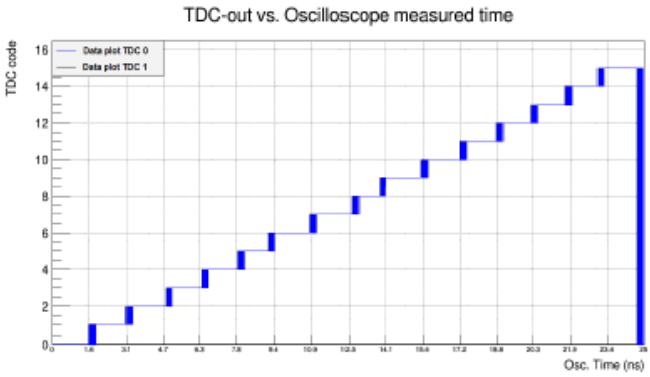

Fig. 5. *Phase measured by scope versus TDC output code.*

In fig. 5 the results of the comparison between the phases measured by the scope and the TDC output is shown. Vertical markers indicate the theoretical bit transition. The plot shows how the TDC changes bit in the correct position all over the range.

In fig. 6 the differences between signal phase measured by the oscilloscope and the TDC are shown. These differences are well centered on zero for the entire range.

In both plots it is evident the wrap around point at the end of the master clock period. In this case the difference between TDC and oscilloscope could be equal to the master clock period.

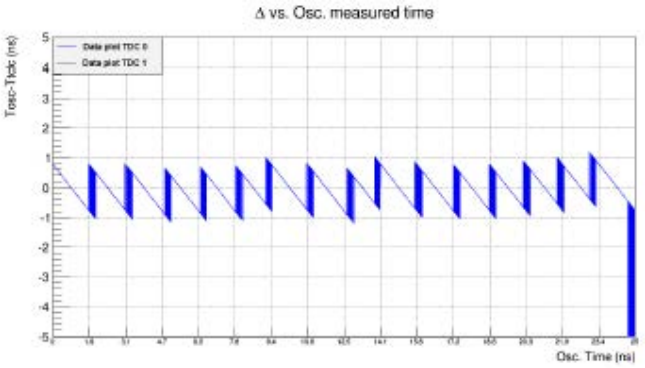

Fig. 6. *Difference between TDC and scope measurements*

IV. Conclusions

We proposed the architecture of a full-digital TDC, based on a synthesizable DCO, which will be used in the new readout chip that is under development for the Muon detector electronic upgrade in LHCb experiment at CERN.

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