Contribution ID: **232** Type: **Poster presentation**

NaNet: FPGA-based Network Interface Cards Implementing Real-time Data Transport for HEP Experiments

Tuesday 7 June 2016 15:00 (1h 30m)

NaNet is a modular design of a family of FPGA-based PCIe Network Interface Cards implementing low-latency, real-time data transport between its network channels and the the host CPU and GPU accelerators memories. The design feature a network stack protocol offloading module that operating in conjunction with a high performance PCIE Gen2/3 X8 core yields a low and predictable communication latency, making NaNet suitable for real-time applications.
A reconfigurable processing module is also available to implement application-specific processing on inbound/outbound data streams with highly reproducible latency.
As of now NaNet design has been specialized in the NaNet-1 (single 1GbE port) and NaNet-10 (four 10GbE ports) configurations employed in the GPU-based real-time trigger of the CERN NA62 experiment, and in the NaNet3 (four 2.5 Gbit optical channels) configuration adopted in the data acquisition system of the KM3NeT-Italia underwater neutrino telescope.
Assessment of the real-time characteristics and performances of the resulting systems will be provided and analyzed.

Authors: LONARDO, Alessandro (Universita e INFN, Roma I (IT)); BIAGIONI, Andrea (INFN); Mrs LO CICERO, Francesca (INFN Sezione di Roma); MARTINELLI, Michele (INFN); Mr FREZZA, Ottorino (INFN Sezione di Roma); Mr PAOLUCCI, Pier Stanislao (INFN Sezione di Roma); VICINI, Piero (Universita e INFN, Roma I (IT)); AMMENDOLA, Roberto (Universita e INFN Roma Tor Vergata (IT))

Co-authors: Mrs PASTORELLI, Elena (INFN Sezione di Roma); LAMANNA, Gianluca (Istituto Nazionale Fisica Nucleare Frascati (IT)); PONTISSO, Luca (Universita di Pisa & INFN (IT))

Presenter: MARTINELLI, Michele (INFN)

Session Classification: Poster session 1

Track Classification: Real Time System Architectures and Intelligent Signal Processing