Intelligent FPGA Data Acquisition Framework

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Abstract—In this paper we present the FPGA-based framework IFDAQ which is used for the development of the data acquisition systems for detectors in high energy physics. The framework supports Xilinx FPGA and provides a collection of the IP cores written in VHDL which use the common interconnect interface. The IP core library offers functionality required for the development of the full DAQ chain. The library consists of the SERDES-based TDC channels, an interface to a multi-channel 80 MS/s 10-bit ADC, data transmission and synchronization protocol between FPGA, event builder and slow control. The functionality is distributed among FPGA modules built in the AMC form factor: front-end and data concentrator. This modular design also helps to scale and adapt the data acquisition system to the needs of the particular experiment. The first application of the IFDAQ framework is the upgrade of the read-out electronics for the straw drift chambers and the electromagnetic calorimeters of the COMPASS experiment at CERN. The framework will be presented and discussed in the context of this upgrade.

I. INTRODUCTION

Data acquisition systems in high energy physics show similar architecture. Most systems use FPGA technology which combines the flexibility in implementing the interface to the detectors, high data throughput and access to external memory. These are necessary features which make FPGA a perfect tool in designing data acquisition systems.

In order to simplify the development of the new systems we attempted to generalize the architecture by unifying communication interfaces, developing re-usable IP cores, and designing generic hardware. The framework is called the Intelligent FPGA Data Acquisition (IFDAQ) and is described in the following section.

II. IFDAQ

The architecture of the framework is shown in fig. 1. The framework contains three types of modules: front-end, data concentrator and trigger generator. The front-end modules are connected to the detector and perform digitization of the incoming signals. The data concentrator modules collect data from the front-ends, combines it into an event and sends the event to the event builder. The trigger generator is used in parallel to the data concentrator. It collects data from the front-ends and uses hit information to generate trigger signal.

A. Front-End

The front-end interface is represented by the TDC core and an interface to the external ADC. The layout of the
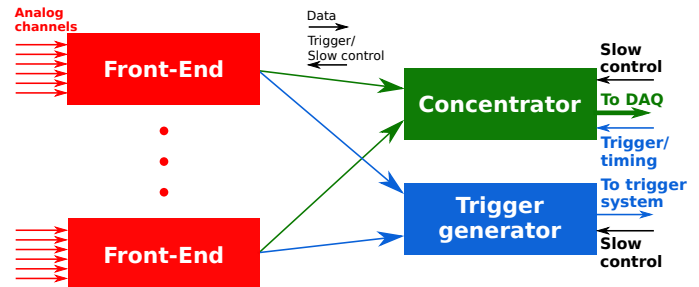
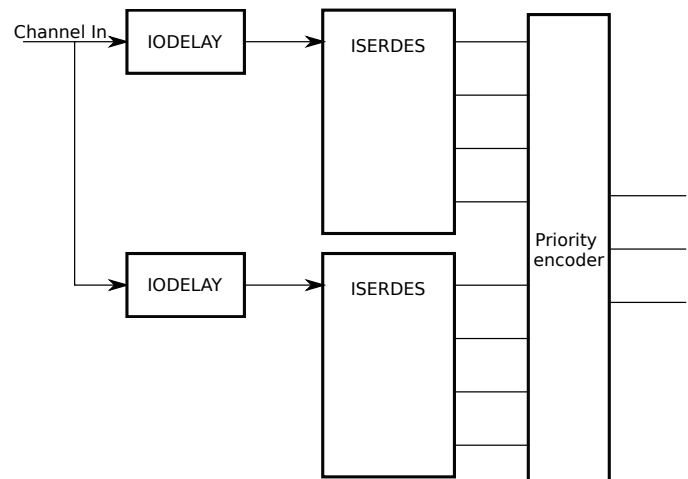Figure 1: Architecture of the IFDAQ framework

Figure 2: Layout of the TDC with 2 ISERDES

TDC is shown in fig. 2. The TDC utilizes hardware FPGA components: serial-to-parallel converter ISERDES and a programmable temperature stabilized delay component IODE-LAY [1]. The TDC is built by connecting 2 or 4 ISERDES/IODELAY pairs to the input signal in parallel. The differences in the signal propagation time to the hardware components are compensated by calibrating the delay in the IODELAY component. The event time is calculated from the deserialized signal by the priority encoder algorithm. Since the priority encoder is the only algorithm implemented in the programmable logic, the footprint of the TDC is extremely small. The theoretical time resolution of the TDC consisting of 2 ISERDES/IODELAY pairs and running with 800 MHz clock in the DDR mode is 100 ps.

The front-end modules can be equipped with external multi-channel sampling ADC of the ADS527x family. The design will follow the structure of the MSADC [2] modules built for the COMPASS experiment. The ADC can work in the interleaved mode thus effectively doubling the sampling fre-
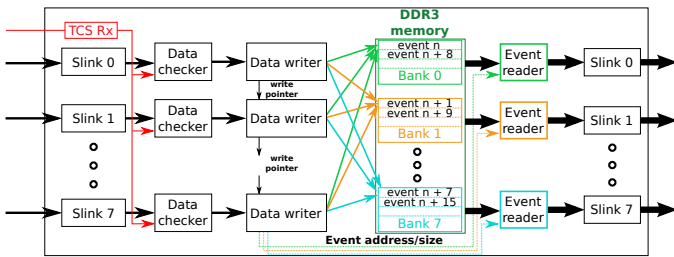
Figure 3: Event builder

quency. An interface core is then implemented in FPGA which performs the serial-to-parallel conversion of the incoming data streams and provisions a serial configuration interface to ADC accessible by the slow control.

B. Communication

The communication between FPGA is done via 3.5 Gb/s high-speed serial links. A new unified communication protocol, UCF, has been developed to unify different communication channels in a single physical link. The UCF protocol provides up to 256 logical channels and guarantees the synchronization of the clock phases. One out of 256 possible channels has a real time priority and may be used to transmit information which requires fixed latency, e.g. for trigger interface. Other channels have lower configurable priority and are used to transmit data and slow control frames.

Additional feature of the protocol is the support for two different topologies The **star topology** reduces the system costs by using the time division multiplexing in the systems with low average data occupancy on the link. The multiple source FPGA are connected to the destination FPGA over a passive optical splitter and therefore only one high-speed link is used on the destination FPGA. The destination FPGA controls the activation and de-activation of the transmitters of the source FPGA using control sequences. The **point-to-point topology** requires one link per source FPGA and is used by the systems with high average occupancy.

The control and configuration of the FPGA is done over IPbus protocol [3]. The IPbus is a UDP-based network protocol which provisions memory-mapped interface to FPGA logic for the control software. The IPbus frames are distributed to the front-end modules via UCF protocol.

C. FPGA-based Event Builder

The event building algorithm has been successfully used in the DAQ of the COMPASS experiment. The algorithm which is shown in fig. 3 is designed around external memory. The memory is divided into banks by the number of the outgoing links. The banks are sub-divided into slots which have a size of the largest possible event and are reserved for single events.

The data received from front-end cards are checked for errors in the data format. The frames with errors in the data format are discarded and replaced with dummy frames which purpose is to preserve the event structure. The first data writer then determines the next bank and writes the event into the new slot. After it finishes it sends the memory pointer to the

next writer and is ready to accept the new event. When the last writer finishes writing the event, the pointer to the event is transmitted to the corresponding memory reader. The reader core then reads the full event and sends it to the outgoing link.

III. UPGRADE OF THE COMPASS READ-OUT ELECTRONICS

The upgrade of the read-out electronics for the electromagnetic calorimeter (ECAL) and the straw drift chambers in the COMPASS experiment will become the first application of the IFDAQ framework. The hardware modules for the upgrade use Artix-7 FPGA and are built in the AMC form factor. The front-end modules for the ECAL carry 4 ADC which can achieve 80 MS/s in the interleaved mode. The front-end modules for the straw drift chambers will be equipped with 64 TDC channels/modules. The concentrator modules are equipped with DDR3 SODIMM socket which can carry up to 4 GB memory modules, high-speed links for communication with the front-end modules and COMPASS DAQ, and an interface to the Trigger Control System.

Front-end boards are installed in microTCA crates where they occupy up to 12 slots. The MCH slots are occupied by 2 interface boards which provision optical fiber transceivers for communication with data concentrator and trigger generator boards in parallel. The concentrator and trigger generator boards are installed in a separate microTCA crate.

IV. SUMMARY

The IFDAQ framework which simplifies the designing of DAQ systems has been developed. Different aspects of the framework have been successfully tested in COMPASS [4] and PENeLOPE [5] experiments as well as in the pixel detector for Belle II [6]. The first application of the IFDAQ will be the upgrade of the read-out electronics for the COMPASS ECAL and straw drift chambers. The IFDAQ framework and its application will be presented in detail in the contribution.

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