A JESD204B-compliant Architecture for Remote and Deterministic-Latency Operation

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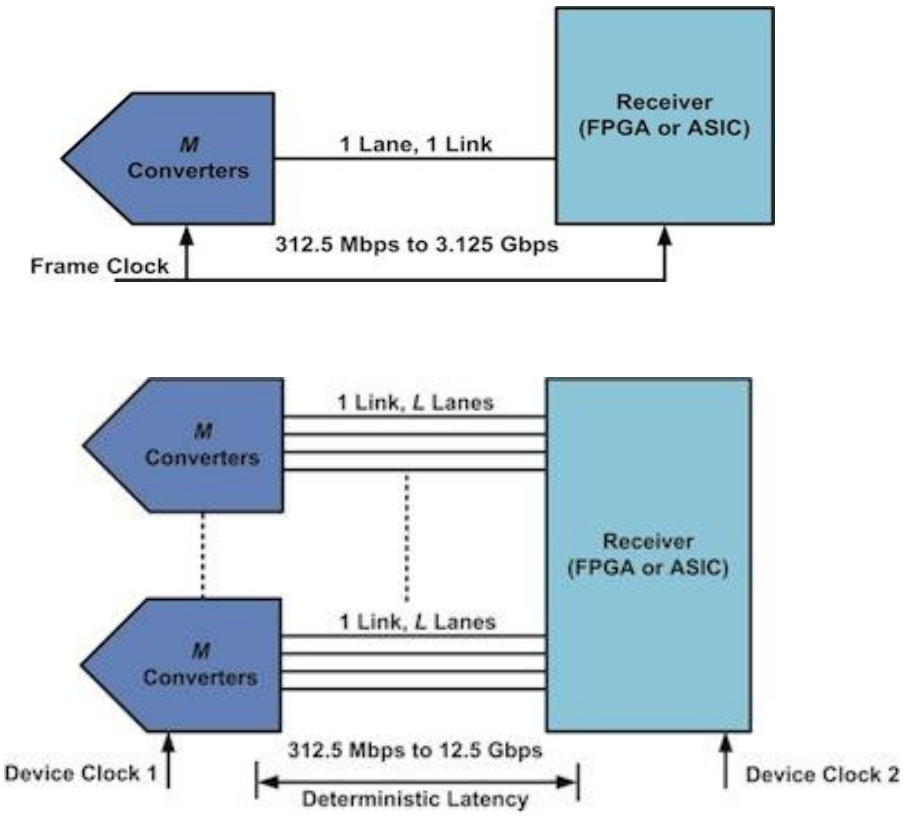
Outline

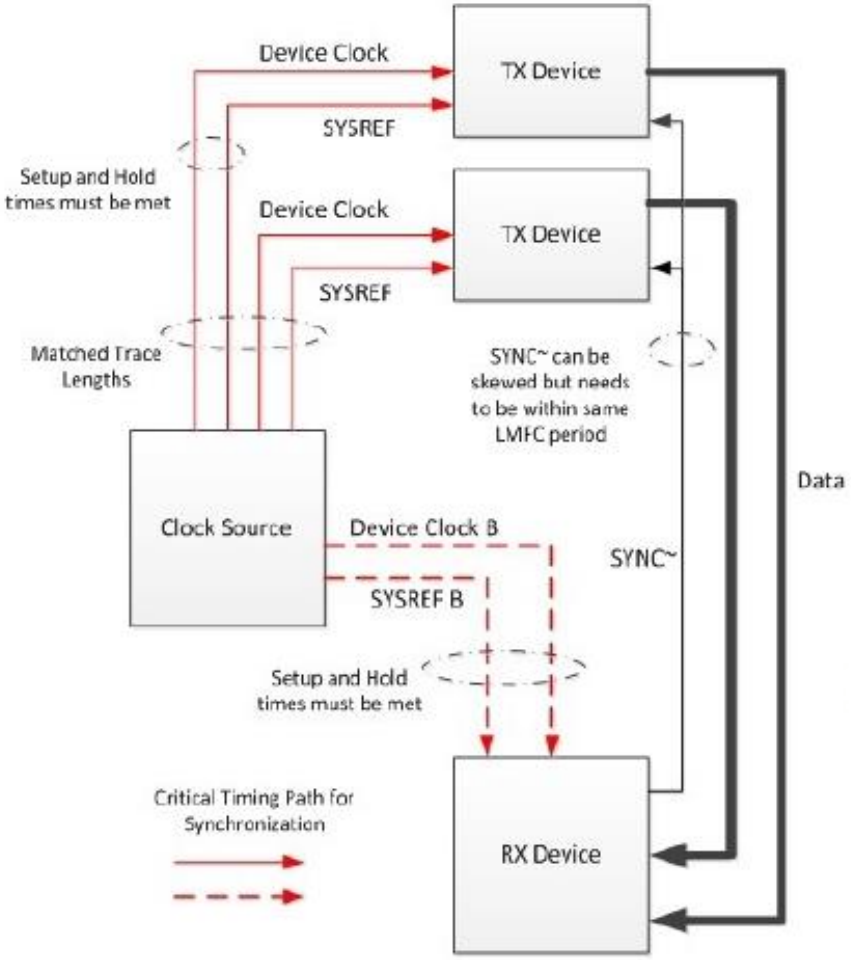
- The JESD204B protocol
- Architecture for remote deterministic-latency readout of JESD204B-compliant devices
- FPGA Prototype
  - Architecture, implementation, logic footprint, jitter on critical clocks
- Conclusions

The JESD204B Protocol

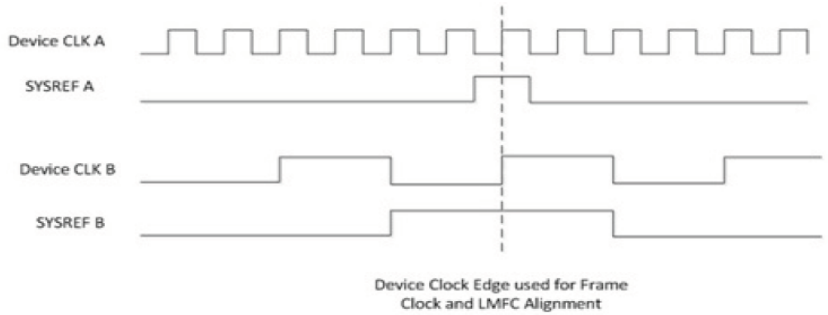


- High-speed interface for data converters (ADCs/DACs)
- 2006, JESD204, single serial lane (released by JEDEC)
- 2008, JESD204A, multiple lanes up to 3.125 Gbps
- 2011, JESD204B, multiple Serial Lanes up to 12.5 Gbps, depending on physical layer, adds deterministic latency (subclasses 1 and 2)
- Aimed at links over distances of few 10cm, Rx and Tx on same board
- Requires dedicated LVDS signals between Tx/Rx in addition to serial lanes

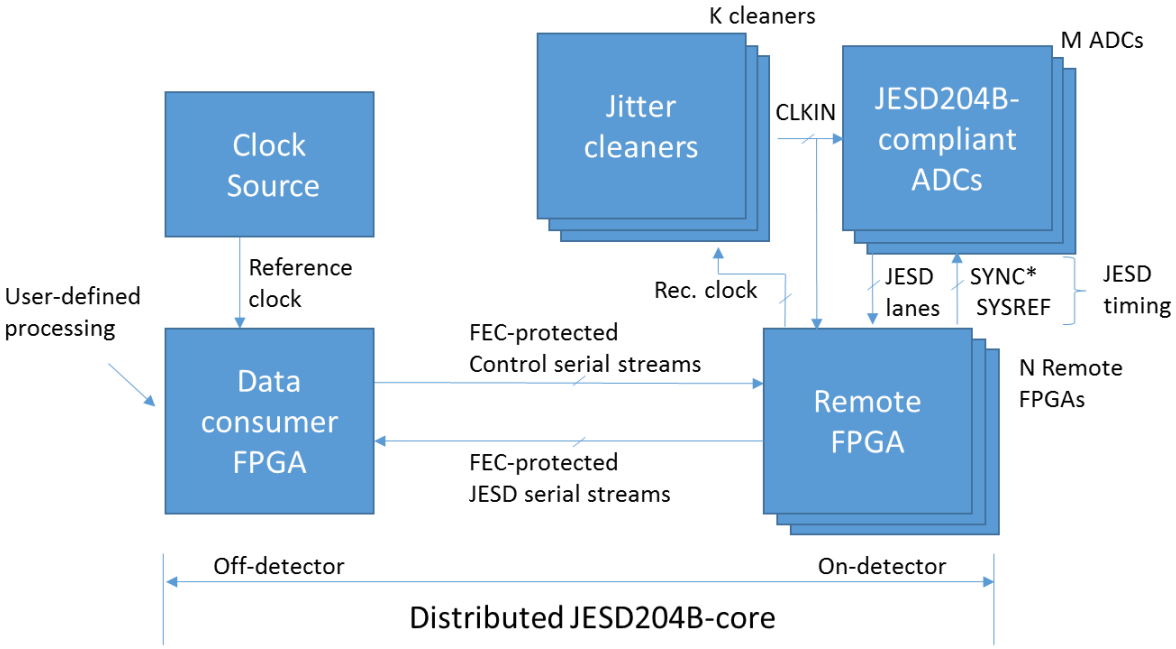
JESD204B Subclass 1



- JESD204B signals
  - serial streams or lanes
  - device clocks (i.e. serial transceivers reference clocks)
  - SYNC* used for Code Group Synchronization (CGS), byte boundary alignment in data link
  - SYSREF used for timing synchronization (unique marking of device clock edges)
    - Synchronous to device clocks



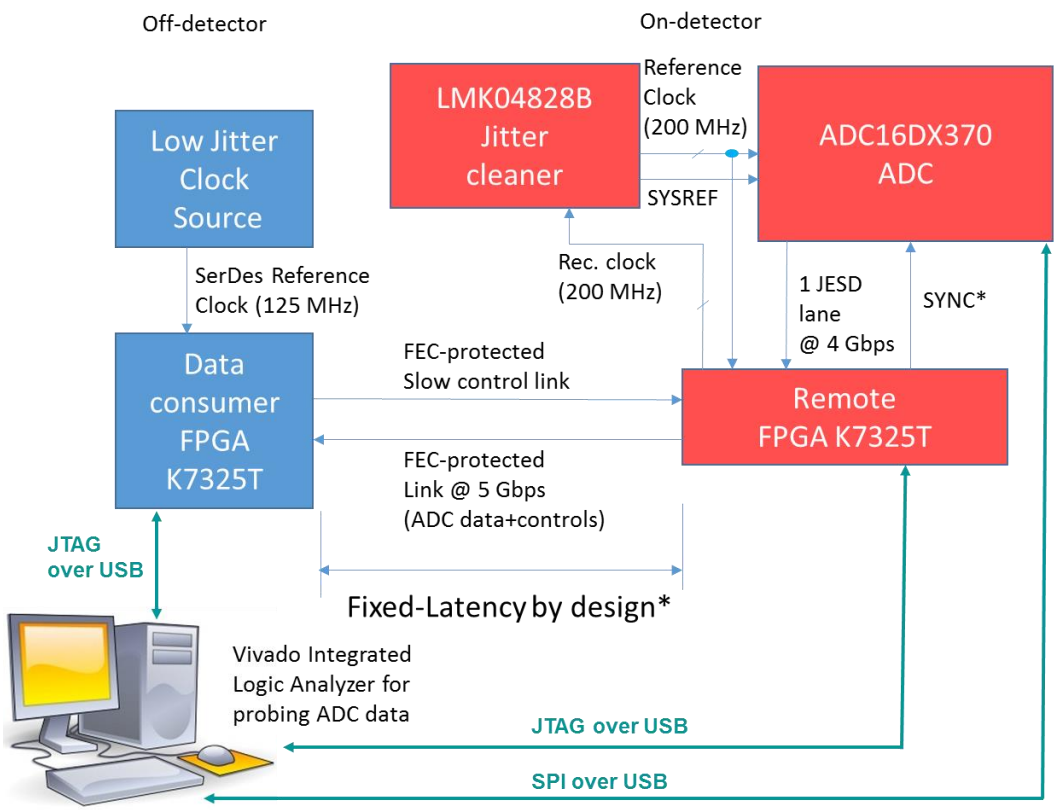
Remote JESD204B Architecture



- 1 local FPGA (data consumer)
- N remote FPGAs connected to M JESD204B-compliant ADCs, handle JESD links

- Forward error correction protected link between local and remote FPGA for enhanced reliability on noisy physical layers (e.g. radiation on detector)
- Bi-directionality ensures slow control IO for configuring converters and jitter cleaners (specific protocol, e.g. I2C, SPI is implemented in Remote FPGA)
- FEC-link includes also a return channel for slow control operations

Demonstrator



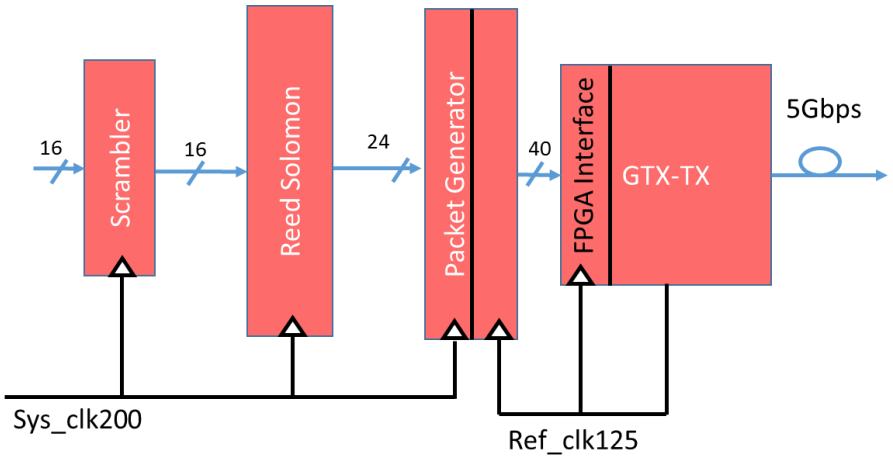
- Firmware in remote FPGA handles JESD complexity (i.e. CGS, ILAS, and alignment monitoring)

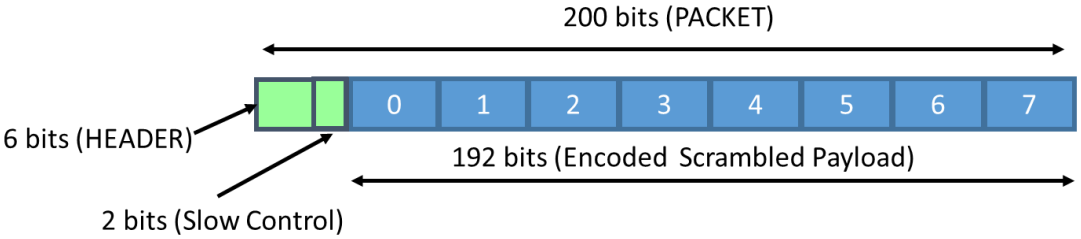
- Simplified implementation of the general architecture: single remote FPGA, single ADC, 1 conversion channel
- Conversion running at 200 MSps, 16bits per sample, TI High-speed ADC (ADC16DX370)
- 1 JESD lane at 4 Gbps
- 1 FEC-protected link at 5 Gbps
  - Embeds ADC data + return channel for slow control
- 1 FEC-protected link at 5 Gbps for sending slow control to remote end, ADC and jitter cleaner configuration
- FEC-link is the only connection between local and remote devices (unlike JESD)

*R. Giordano and A. Aloisio, "Fixed-Latency, Multi-Gigabit Serial Links With Xilinx FPGAs," in IEEE Transactions on Nuclear Science, vol. 58, no. 1, pp. 194-201, Feb. 2011. doi: 10.1109/TNS.2010.2101083

FEC-Protected Link Remote Tx

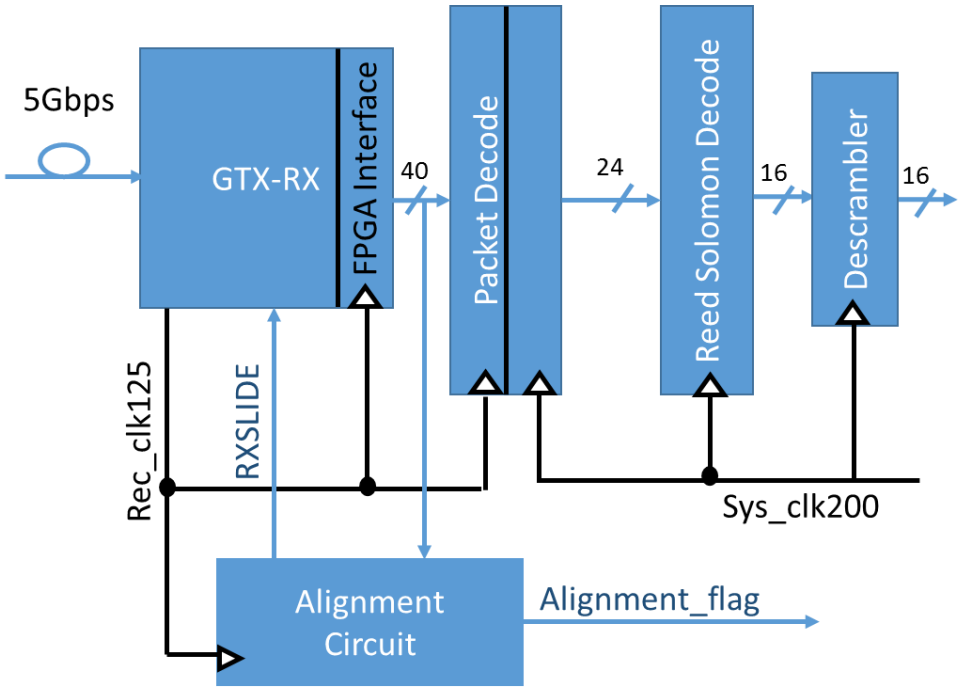
- Parallel input 16 bits words (ADC data)
- Scrambled and Reed-Solomon (6,4) encoded, 4-bit symbols, 16bits =>24bits
- Packet builder
  - assembles 8 24-bit words
  - adds alignment header (6 bits) and slow control (2 bits)
- 200-bit packet is split into 5 40-bit words to fit GTX transceiver parallel word size





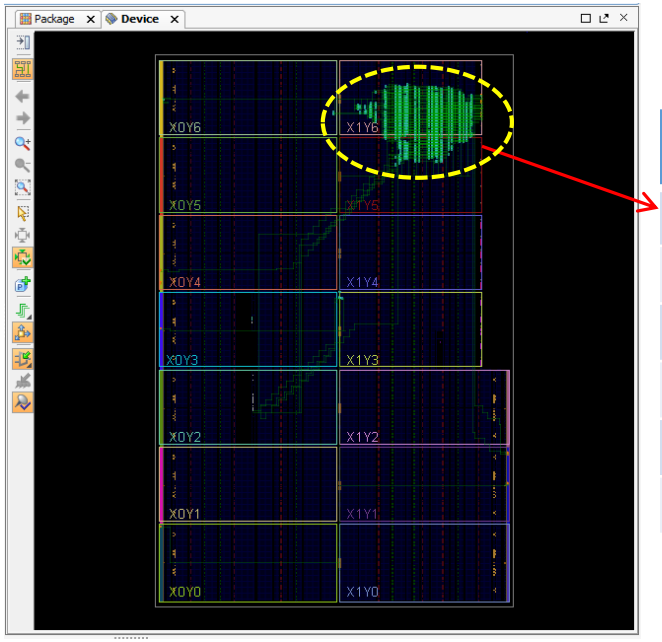
FEC-Protected Link Local Rx

- Alignment circuit searches for headers to determine packet boundary
- Payload is then unpacked, RS-decoded and descrambled
- RS can correct up to 32 bit errors per packet



FPGA Implementation

Xilinx Kintex-7 325T



JESD-Link (1 lane)

Logic Resources	Used/Available	Percentage
Registers	3901/407,600	1%
LUTs	3263/203,800	2%
BlockRAM	2/445	1%
BUFGs	5/32	15%
BUFGDS_GTEs	1/8	12%
GTXs	1/16	16%

FEC-Link (Tx+Rx)

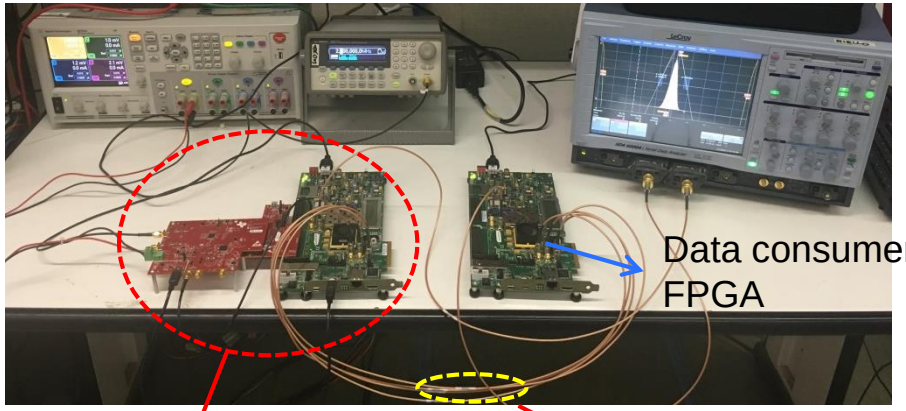
Logic Resources	Used/Available	Percentage
Registers	6,820/407,600	1%
LUTs	5,082/203,800	2%
FIFOs	6/445	1%
BUFGs	5/32	15%
BUFGDS_GTEs	1/8	12%
GTXs	1/16	16%

- Overall logic footprint occupation for both JESD and FEC link is tiny (2% per JESD lane + 2% per FEC link)
- small FPGA could be employed on detector
- Available transceivers are the actual limit

Test setup

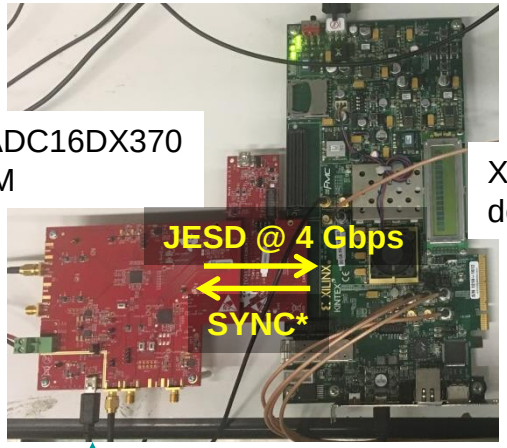
4V Power Supply For ADC EVM

Test signal generator



Remote FPGA + ADC

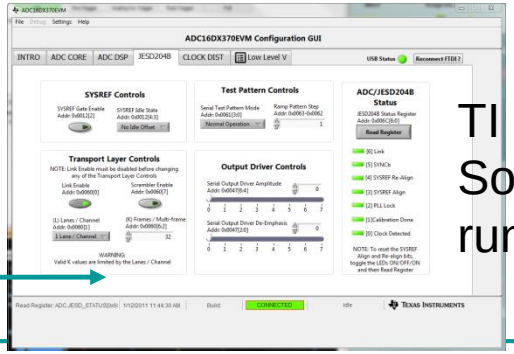
5 Gbps FEC-protected fixed-latency links



TI ADC16DX370 EVM

Xilinx Kintex-7 demo board (KC705)

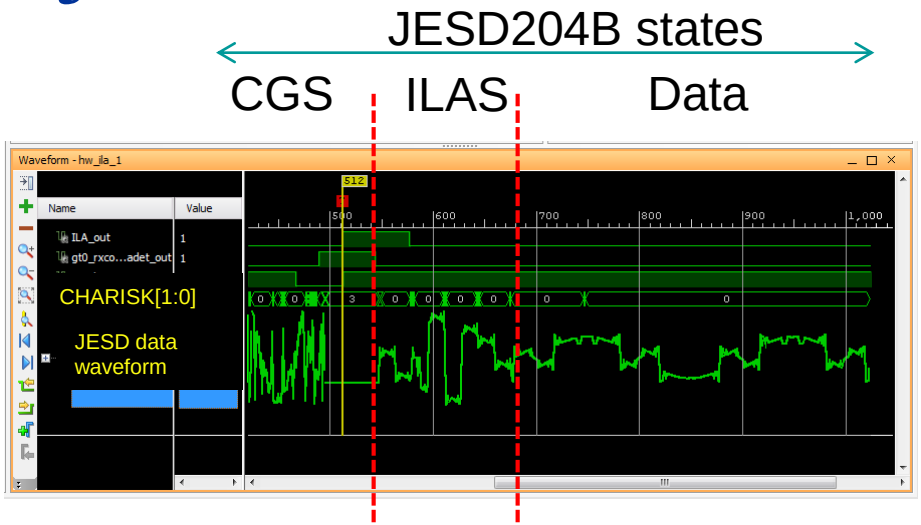
SPI over USB



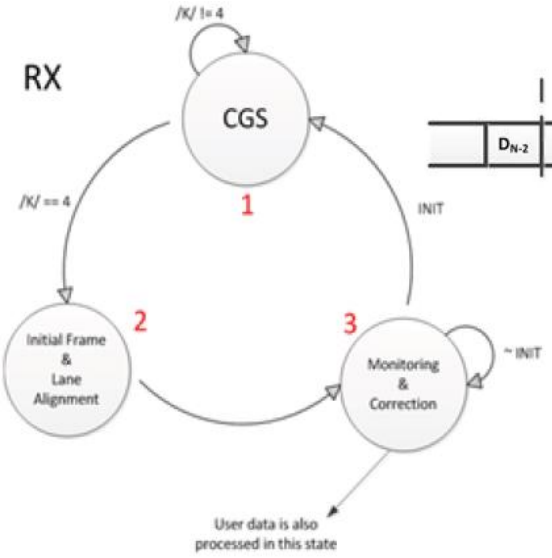
TI configuration Software running on PC

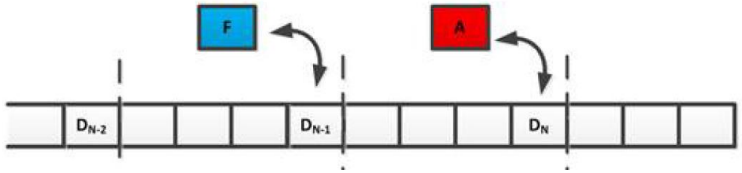
- Pair of Xilinx KC705 demo boards
- FEC-protected links routed on 50Ω coax cable pairs
- TI eval board w/ ADC and jitter cleaner plugged on KC705, via FMC connector
- ADC and Jitter cleaner configured via SPI over USB connection on TI board
- Tested functionality
- Measured jitter on recovered clock and on reference clock for remote JESD link

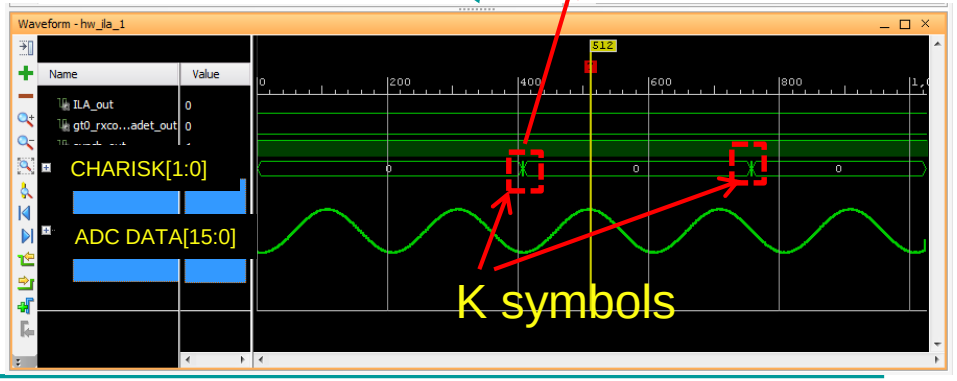
JESD204B Link: Test Results



- JESD Link
  - Hardware test with Xilinx Vivado Hardware manager, virtual input output + integrated logic analyser
  - JESD data arranged in multiframes (sequence of K frames)
  - ADC replaces last octet of a frame (D_n) if $D_n=D_{n-1}$ with /A/ or /F/ 8b10b K symbols
  - In Rx, alignment monitor checks /A/ and /F/ at expected positions and restores data



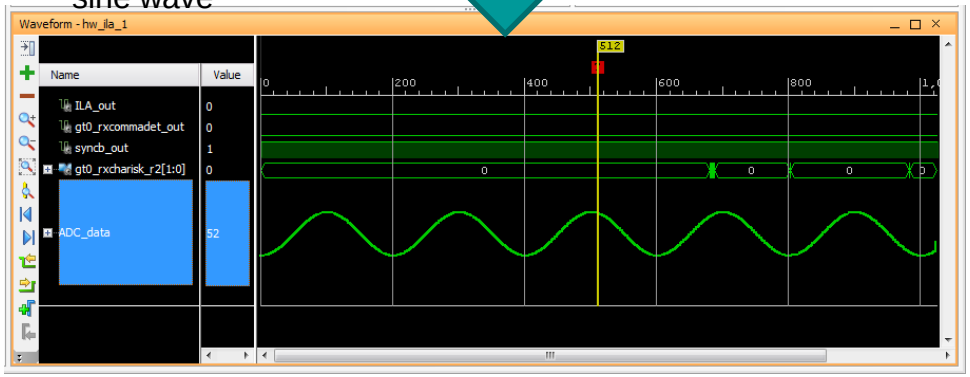




JESD204B Link: Lessons Learned

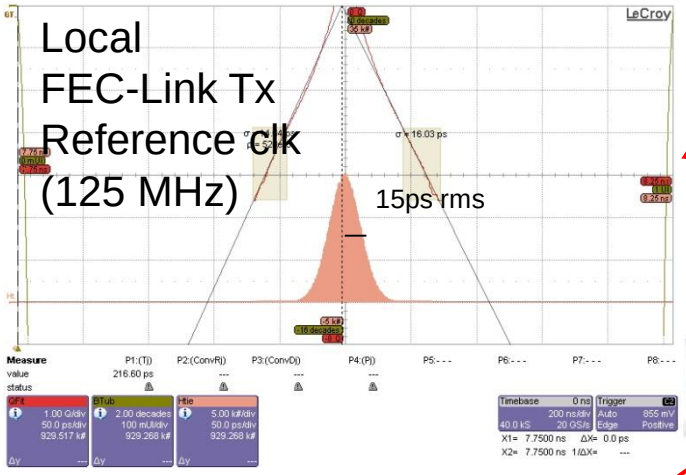
Test signal:
1 MHz, 800mV
sine wave

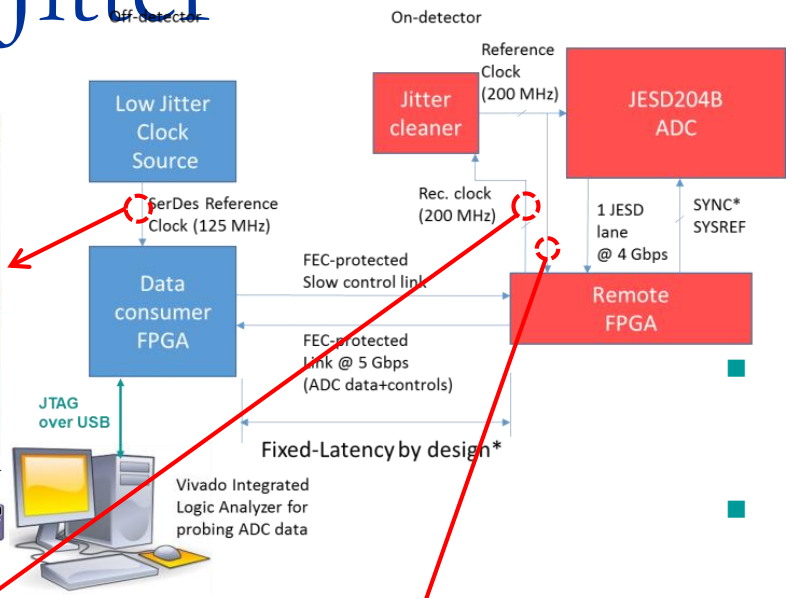
Decoding

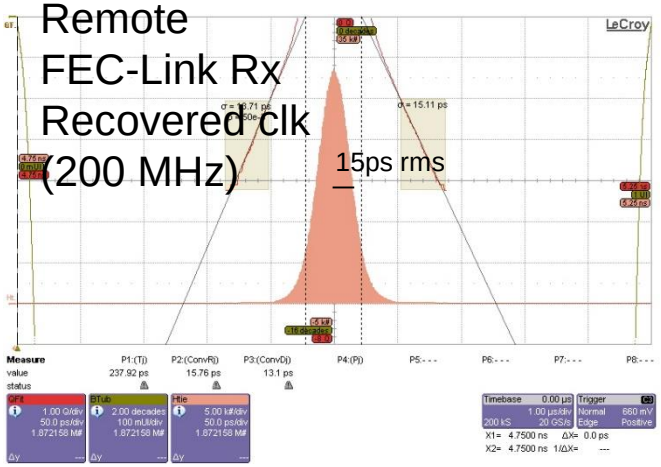


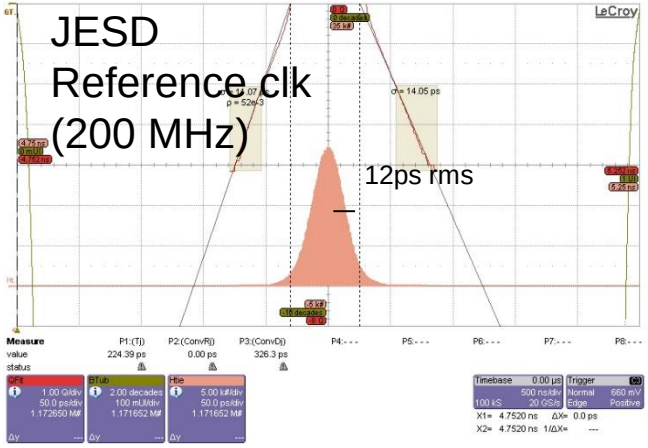
- /F/ (K28.7) characters used for replacement on frame boundaries contain a comma
- Comma detection must be disabled after CGS (which includes /K/ K28.5) otherwise misalignment might happen
- Octects from ADC16DX370 are encoded (not scrambled!)

Device Clock Jitter









- Scope running jitter analysis software
- For all clocks, negligible deterministic jitter
- Comparative results
- All clocks are probed through the FPGA on KC705, i.e. actual jitter is better!

Conclusions

- Developed simple and light JESD204B-compliant core
- Tested with a single lane running at 4 Gbps (200 MSps 16-bit conversion)
- Developed a FEC-protected, deterministic-latency 5 Gbps link for transferring conversion data toward a remote data consumer
- The whole data transfer path features deterministic latency
- JESD204B might be tricky (misalignment, device might require user data decoding)
- This work is part of the Scientific Independence of young Researchers (SIR) ROAL project funded by the Italian Ministry of Education, University and Research (MIUR) in 2014
- I thank the Conference organizers for allowing me to change the schedule of my talk