A JESD204B-compliant Architecture for Remote and Deterministic-Latency Operation

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***Abstract*—High-speed analog-to-digital converters (ADCs) are key components in a huge variety of systems, including trigger and data acquisition (TDAQ) systems of Nuclear and Sub-nuclear Physics experiments. Over the last decades, the sample rate and dynamic range of high-speed ADCs underwent a continuous growth and it required the development of suitable interface protocols, such as the new JESD204B serial interface protocol.**

In this work, we present an original JESD204B-compliant architecture we designed, which is able to operate an analog-to-digital converter in a remote fashion. Our design includes a deterministic-latency high-speed serial link, which is the only connection between the local and remote logic of the architecture and which preserves the deterministic timing features of the protocol. By means of our solution it is possible to read data out of several converters, even remote to each other, and keep them operating synchronously. Our link also supports forward error correction (FEC) capabilities, in the view of the operation in radiation areas (e.g. on-detector in TDAQ systems).

We discuss an implementation of our concept in a latest generation FPGA (Xilinx Kintex-7 325T), its logic footprint, frequency performance and power consumption. We present measurements of the timing jitter and latency stability of JESD204B timing-critical signals forwarded over the link. We also describe a demo application of our architecture.

***Index Terms*—Digitally controlled oscillator, ASIC, FPGA.**

I. Introduction

HIGH-SPEED analog-to-digital converters (ADCs) are key components in a huge variety of systems, such as wireless infrastructure transceivers, software defined radios, radar, secure communications, medical imaging systems and trigger and data acquisition (TDAQ) systems of Nuclear and Sub-nuclear Physics experiments. In fact, the usage of high-speed ADCs for digitizing analog pulses produced by the front-end electronics [1,2,3,4] opens the way to a fully digital processing, which can be implemented by means of application specific integrated circuits (ASICs) or field programmable gate arrays (FPGAs). Over the last decades, the sample rate and bit dynamic of high-speed ADCs underwent a continuous growth. In order to keep pace with the needed output data rate, the digital interface of devices evolved from traditional parallel single-ended CMOS, which offered bandwidth of the order of 100Mbps, to serial low voltage differential signaling (LVDS), which increased the bandwidth up to 1Gbps, at the cost of a higher power consumption. Anyway, both CMOS and LVDS interfaces required the routing of multiple traces printed circuit board (PCB) from the converter to the data processor. In order to overcome bandwidth limitations and to simplify the PCB routing, the Joint Electron Device Engineering Council (JEDEC) has proposed a new, serial interface protocol (JESD204B [5]) optimized for analog-to-digital and digital-to-analog converters. The JESD204B standard supports data rates of up to 12.5Gbps per serial lane and foresees dedicated features to guarantee a deterministic timing of the conversion and to support the synchronization of multiple converters in the same system. The portfolio of JESD204B-compliant converters is in constant growth and FPGA vendors and third parties offer intellectual properties for handling the protocol complexity (e.g. [6, 7, 8, 9]). The timing predictability of the protocol is of great interest for TDAQ systems, where it is often required to operate the whole apparatus synchronously in order to preserve critical trigger information and timing-related data. It is important to note that the JESD204B standard is designed for local operation, i.e. the data producer and consumer chips are meant to be on the same board or anyway at distances of the order of few centimeters, while TDAQ systems may require the converter to be remote (e.g. on-detector) with respect to the logic receiving the data (e.g. off-detector).

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II. System Architecture

In this work, we present an original JESD204B-compliant architecture we designed, which is able to operate an analog-to-digital converter in a remote fashion. Our design includes a deterministic-latency high-speed serial link, which is the only connection between the local and remote logic of the architecture and which preserves the deterministic timing features of the protocol. By means of our solution it is possible to read data out of several converters, even remote to each other, and keep them operating synchronously. Our link also supports forward error correction (FEC) capabilities, in the view of the operation in radiation areas (e.g. on-detector in TDAQ systems). We discuss an implementation of our concept in a latest generation FPGA (Xilinx Kintex-7 325T [10]), its logic footprint, frequency performance and power consumption. We present measurements of the timing jitter and latency stability of JESD204B timing-critical signals forwarded over the link. We also describe a demo application of our architecture with a high-speed ADC [11] running a 16-bit dual channel conversion at 200 Msps corresponding to a line rate of 4 Gbps. This work is part of the ROAL project funded by the Scientific

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