A 3.9 ps RMS Resolution Time-to-Digital Convertor Using Dual-sampling Method on Kintex UltraScale FPGA

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***Abstract*–The principle of tapped-delay line (TDL) style field programmable gate array (FPGA)-based time-to-digital converters (TDC) requires finer delay granularity for higher time resolution. Given a tapped delay line constructed with carry chains in an FPGA, it is desirable to find a solution subdividing the intrinsic delay elements further, so that the TDC can achieve a time resolution beyond its cell delay. In this paper, after exploring the available logic resource in Xilinx Kintex UltraScale FPGA, we propose a dual-sampling method to have the TDL status sampled twice. The effect of the new method is equivalent to double the number of taps in the delay line, therefore a significant improvement in time resolution should present. Two TDC channels have been implemented in a Kintex UltraScale FPGA and the effectiveness of the new method is investigated. For fixed time intervals in the range from 0 to 440 ns, the average time resolutions measured by the two TDC channels are respectively 3.9 ps with the dual-sampling method and 5.8 ps by the conventional single-sampling method. In addition, the TDC design maintains advantages of multichannel capability and high measurement throughput in our previous design. Every part of TDC, including dual-sampling, code conversion and on-line calibration could run at 500 MHz clock frequency.**

I. Introduction

THE basic principle implementing a time-to-digital convertor (TDC) on a field programmable gate array (FPGA) is using a time counter and a time interpolator to provide a coarse timestamp and a fine timestamp respectively for a hit signal. The commonly used time interpolator is tapped-delay lines (TDL), which are constructed by cascading the internal carry chain originally designed for arithmetic circuit (Fig. 2). The intrinsic delay values between taps determine the time resolution of TDC. Because the status of the delay line is sampled by a bank of Flip-flops at system clock, the TDC bin width has two main contributions: one is the physical transmission delay along the path between two taps, the other is the clock skew presented at the flip-flops to register the TDL status. Since the pre-defined FPGA resource is not specifically provided for TDC delay line, these two factors normally make TDC bin widths with a large variation, even negative or zero bins presented. In order to improve the time resolution, these negative and zero bins must be corrected and reused by the bins realignment method, which was introduced in our previous work [1].

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Normally, an FPGA manufactured with more advanced processing technology will have smaller intrinsic delay elements. To improve the time resolution beyond the cell delay, it is highly desirable finding a solution, such as Wave Union method, to subdivide the delay cell further. During our exploration using Xilinx Kintex UltraScale FPGA, which is manufactured by 20 nm processing technology, for high time resolution, we found the logic resource in this family suitable for the implementation to sample the single TDL status twice. In this paper, we are building the TDC channels with this new dual-sampling method. The effect of the new method is equivalent to double the number of taps in the delay line, which will largely improve the time resolution. The test results show that the dual-sampling method could improve time resolution from 5.8 ps to 3.9 ps. Furthermore, the dual-sampling design maintains advantages of multichannel capability and high measurement throughput in our previous design. Every part of the on-line TDC can run at 500 MHz clock frequency, which demonstrates the practicability of our new method.

II. Implement of Dual-sampling Method

A. TDC Architecture

The TDL is constructed by connecting the carry logics in each logic slice, and cascading the slices. After a hit signal comes, a rising edge will propagate on the carry chain. The state of carry chain will be captured into registers when the rising edge of system clock comes as shown in Fig. 1. As many bubbles exist, the original output code is like 00010111. After a switch by the realignment fabric, the code is conversed to 00001111, which is a pure thermometer code. The thermometer code then is encoded to one hot code like 00001000, which is encoded to binary code like 100. The binary code is sent to calibration circuit to do a bin-by-bin calibration. After calibration, the fine time stamp is got, which forms time stamp of a hit signal together with coarse time stamp.

B. Bin Realignment

More than half of the bins are negative and zero width, which results from the inhomogeneous delay taps and the clock skew differences on the clock distribution tree. To reduce them, we can realign the bins by switching the position of the registered status. That is, to reduce bubbles, we map the physical position sequence of the tap to time arriving sequence [1]. By bin realignment process, almost all the bins have some values and the variation of bin width turns small.

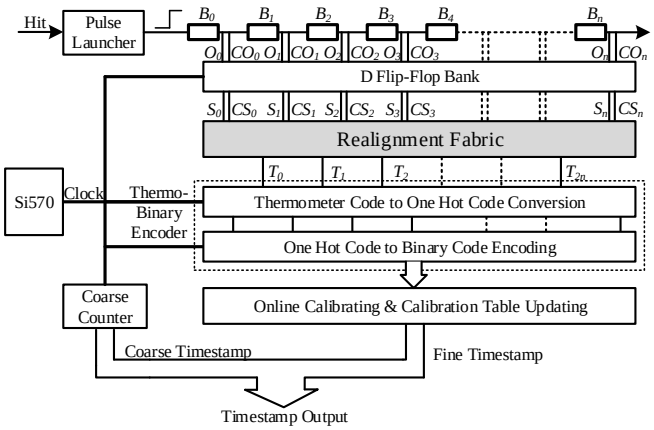

Fig. 1. Diagram of function blocks in a TDL-TDC.

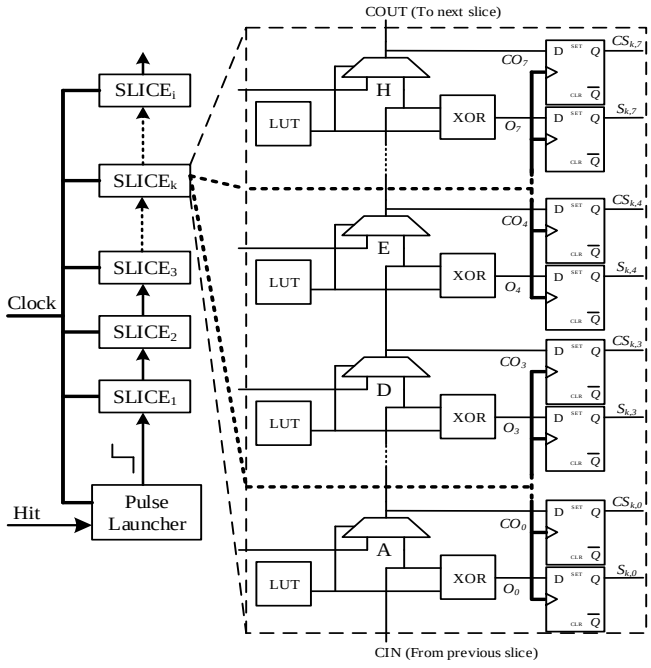

Fig. 2. Using the carry chain in the Kintex UltraScale FPGA to construct the tapped-delay line

C. Dual-Sampling Method

Fig. 2 shows the slice structure of Kintex UltraScale FPGA. Unlike slice structure of Xilinx 6-serials or 7-serials FPGA that only one output of each tap can be captured by register in the same slice, the two outputs of each tap in Kintex UltraScale can be captured in the same slice. For a definite system clock, the length of carry chain is also definite. By capturing both output of the carry chain, we can halve the bin width with the same length of carry chain. In our design, the frequency of system clock is 500 MHz, the length of carry chain is 430, so the average bin width is 4.65 ps. When the dual-sampling method is used, the average bin width will be 2.33 ps. Number of original bubbles will increase after capturing both output, which makes realignment process more necessary. Fig.3 shows the bin width distribution after realignment process with dual-sampling method. Only several bin width is above 10 ps and almost no bubble exists anymore.

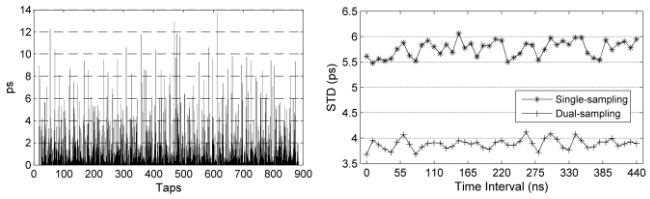

Fig. 3. (a) Bin width of dual-sampling TDC after bin realignment. (b) RMS resolution of dual-sampling TDC and single-sampling TDC.

The RMS test shows that the single-sampling TDC gets a 5.8 ps RMS resolution, the dual-sampling TDC gets a 3.9 ps RMS resolution. The dual-sampling resolution is approaching the theoretical value of $5.8/\sqrt{2}$=4.1 ps.

III. Test Results

A. The Measured Bin Width

The dual-sampling TDC was implemented on the developing board KCU105. Using the code density method, the actual distribution of the bin width after the bin realignment is measured and shown in Fig. 3(a). Within 2 ns clock period, hit signal go through the carry chain from bin 17 to bin 885, which means the average bin width captured out by dual-sampling method is 2.3 ps.

B. RMS Time Resolution

Two same TDC channels were implemented. As a contrast, we implemented both single-sampling TDC and dual-sampling TDC. The hit signals for TDC were generated by the arbitrary waveform generator AWG5012C from Tektronix. The time interval between the hit signals was adjusted by setting the phase difference between the two output channels, which was set at about 10 ns. The hit signals initiated the TDCs to record both the coarse timestamps and the fine timestamps, which were then readout via the UART interface on the developing board. The test result in Fig. 3(b) shows that the RMS resolution of dual-sampling TDC is 3.68 ps to 4.12 ps with an average value of 3.9 ps and the single-sampling TDC is 5.48 ps to 6.06 ps with an average value of 5.8 ps within our tested time interval in range from 0 to 440 ns.

IV. Conclusion

The Xilinx Kintex UltraScale FPGA manufactured by 20 nm process has small delay granularity. The new slice structure make dual-sampling possibility. The dual-sampling method has a good effect to divide bin width only with the cost that more capturing resisters and a bigger encoder module are needed. The realignment method is effective to map the physical position sequence to time sequence which reduces the demand for bubble proof, gets rid of bubble error and improves resolution. With a 500 MHz clock used, the total resource occupied by each TDC channel is not too much, which makes implementing multichannel on a single FPGA available.

References

[1] C. Liu, Y. Wang, “A 128-Channel, 710 M Samples/second, and Less than 10 ps RMS Resolution Time-to-Digital Converter Implemented in a Kintex-7 FPGA”, IEEE Transactions on Nuclear Science, Vol.62, No.3, JUNE 2015, pp773-783.