High Speed Ethernet Application for the Trigger Electronics of the New Small Wheel

Houbing Lu, Kun Hu, Xu Wang, Feng Li, Liang Han, and Ge Jin

Abstract–**The ATLAS detector will be upgraded in 2018. The main focus of the Phase-I ATLAS upgrade is on the Level-1 trigger, replacing the present muon small wheels (SW) with the "new small wheel(NSW)", which consists of small thin gap chamber(sTGC) and micromegas (MM). A versatile application-specific integrated circuit(ASIC), the VMM chip, have been developed to read out the signals of the sTGC and MM. The VMM have 64 channels. In order to test the performance of the VMM, a large data transfer rate is needed. Meanwhile, it is required to implement the multi-board interconnection. It is proposed to apply the high-speed Ethernet-based network. We designed and implemented a test platform, the Gigabit Ethernet Module(GEM). The test result shows that the transfer rate can reach up to 926Mbps. Subsequently, the Ethernet is applied in the pad front end board (pFEB) and the thin gap chamber simulation signal generator (SG). This paper introduces the implementation of the GEM platform, as well as its applications. The features of the systems are described in detail.**

I. Introduction

ATLAS[1] is one of four experiments that is located at the Large Hadron Collider (LHC) now being constructed at CERN, Geneva, Switzerland. The ATLAS detector accepts the events from the proton–proton collision at a rate of 40 MHz. The Tracks containing events of interest are selected via a series of trigger decisions. At high luminosity, the performance of the muon tracking chambers, both in terms of efficiency and resolution, degrades with the increase of the background rate, especially in the end-cap region. Moreover, the low energy protons, generated in the materials between the SW and the end-cap muon detector, hits the end-cap trigger chambers, thus producing fake triggers. In order to cope with these problems, it is proposed by ATLAS collaboration to replace the current muon SW with the NSW. The thin gap chamber (TGC) technology, developed in 1983, is an important part of the SW. The sTGC[2] in which the strip pitch is much smaller than that of the current ATLAS TGC will be applied for the upgrade of the NSW. Each sTGC detector consists of four pad-wire-strip planes. The pads are used through a 3-out-of-4 coincidence to identify muon tracks approximately pointing to the interaction point. are also used to determine which strips need to be read out to obtain a precise position measurement in the precision coordinate. The charges of the wires are read out to obtain the azimuthal coordinate of a muon trajectory.

An application-specific integrated circuit (ASIC) (the so-called VMM chip[3])is being developed to read out the pads, strips and wires of the sTGC detectors. The current version, the VMM2[4] chip, is able to read out both positive (strips, pads) and negative (wires) polarity signals, on 64 individual readout channels. The pad trigger rate in the Level-1 is of order 40MHz. Fortunately, not all channels of the VMM accept the events simultaneously. However, the high speed data transfer interface is also required to send out the events from the sTGC. For the multiple sTGCs, the one-to-many interconnection of the front end board (FEB) is needed. Therefore, the network is the best option.

In this paper, we will introduce a high-speed test platform, the gigabit Ethernet module (GEM). The WinPcap[5] (windows packet capture) technique is used to achieve the communication between the hardware and the computer. The performance of the gigabit Ethernet, including number of lost packets, reliability, and transfer rate, is described below. Subsequently, we apply the high speed Ethernet to pFEB and SG. The results are presented in detail.

II. GEM Implementation

The GEM provides a test platform for the Ethernet. In the following we describe the architecture of the GEM, this new platform is fully programmable and delivers Gigabit wire-speed performance.

A. Hardware and Firmware

The standard TCP/IP communication protocol are very complex and large, it's hard to implement on FPGA. Hence we adopt the MAC(media access control) protocol, which can be implemented on a FPGA device. That is a technology to realize direct access and transfer of the data in the FIFO of FPGA from the computer. All processing is done in the hardware, no processor is necessary enabling it to achieve high speed data transfers, which is specifically designed to simplify the communication with front-end device. In other word, the communication and data transmission between PC and GEB is entirely taken care automatically by the custom protocol on FPGA. This significantly simplifies the development of the network or any further upgrades, user needs only to concern with providing proper read and write flags for the data transferring to work.

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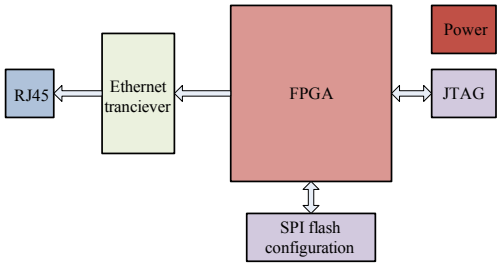

Fig. 1. The schematic block diagram of the GEM.

The schematic block diagram of the GEM is illustrated in Fig. 1. The core of the GEM is based on a Kintex-7 FPGA[6], which is configured by a serial peripheral interface flash. In order to simplify the hardware design, the Ethernet MAC core is embedded in the FPGA for implementation of Ethernet data link layer. The functionality of the MAC is well defined and fixed for Ethernet protocol. For this reason, the Xilinx Gigabit Ethernet MAC core is used for the this design. In order to have an Ethernet connection, physical layer uses PHY device, and connect PHY device to the FPGA. The Ethernet transceiver with the 1000BASE-T standard is operated at the physical layer. The Alaska 88E1111 Gigabit Ethernet Transceiver is a physical layer device used this containing a single Gigabit Ethernet transceiver and supports the GMII, and the Alaska 88E1116R Gigabit Ethernet Transceiver is a physical layer device used this containing a single Gigabit Ethernet transceiver and supports the RGMII (Reduced pin count GMII), they can direct connection to the Gigabit MAC core block. The RJ45 port implements the connection between the hardware and the computer.

Xilinx FPGA provides an optimized TEMAC IP[7] core, one can for instance deploy the Xilinx Core generator to configure and generate TEMAC wrapper files that contain a user configurable Ethernet MAC physical interface, e.g., GMII, RGMII. Xilinx also provides an scheme for the physical interface as well as a simple FIFO-loopback example design which is connected to the TEMAC client interface.

Although the TEMAC wrapper files greatly simplify the usage of the TEMAC, Users still need to improve the wrapper according to the needs of the project, and extra logic is required to replace the FIFO-loopback example design, and also allows for encapsulating user packets with custom protocol by using a very small fraction of hardware resources. Fig. 2 shows TEMAC functional block diagram.

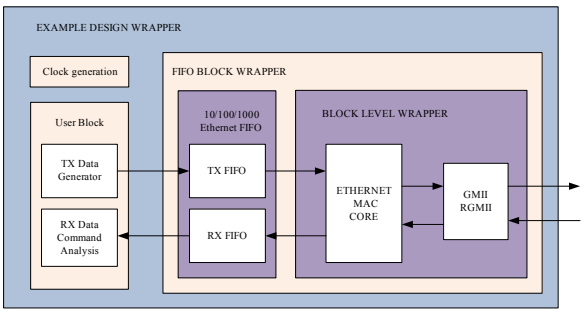

Fig. 2. TEMAC functional block diagram.

The design includes a basic glue logic brings up the external PHY and MAC to allow basic frame transfer or receive. A TX Data Generator and RX Data Command Analysis are also included. With the User Block replacing the loopback demonstration, where Loopback functionality is provided as either MAC RX to TX loopback, or PHY TX to RX loopback, to implement our design, Basic control of the state machine, allowing User Block interface to FIFO Block Wrapper easily.

B. Software Framework

Applications for network analysis rely on an appropriate set of primitives to capture packets, monitor the network and more. The communication between the servers and the clients is done using the MAC protocol now, Windows capabilities are not satisfying for it is not a standard TCP/IP communication protocol where all computer adopt. so we use WinPcap technology to capture Ethernet packets. WinPcap is the industry-standard tool for link layer network access in Windows environments. WinPcap consists of a driver, which provides low-level network access to capture and transmit network packets directly and bypass the complexity of TCP/IP protocol stack. WinPcap architecture consists of three parts as is shown in Fig. 3.

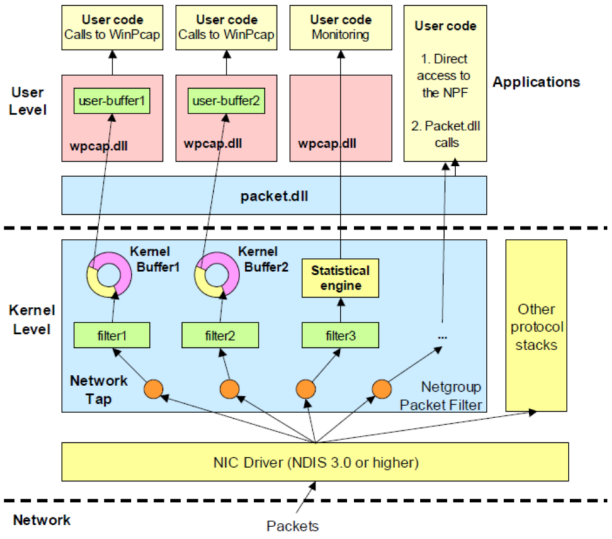

Fig. 3 Structure of WinPcap.

The basic structure of WinPcap retains some most important modules: a filtering machine, two buffers (kernel and user) and a couple of libraries at user level. WinPcap includes an optimized kernel mode driver, called Netgroup Packet Filter (NPF), which directly interact with the network card drivers to get on the network transmission of the original data packet. Its function is to filter data packets and transmit the data packet to user-level perfectly. Packet.dll, offering a system-independent API, provide a common interface to the packet driver among the Win32 platforms. Pactet.dll can perform low-level operations such as obtaining the name of adapter, dynamic loading driver and some system-specific information of the machine and hardware. WPcap.dll, is Operation System-independent, contains some high-level

functions such as filter generation, user-level buffering, statistics and packet injection, which one can easily use.

SG and pFEB serves as server, We are using a fast implementation of the MAC protocol which uses only one client connection per session. and The GEM client utilize Windows and a Visual Studio application which is responsible for the configuration, constant monitoring of the cards, and the handling of connections to servers. The GEM client application runs on any machine with a C++ interpreter. On the client side, each of the two GEM boards is seen as an individual entity with different MAC address. The physical location of a GEM board is completely transparent to the user, The entire system is controlled from the client PC (personal computer). A graphical user interface is available for displaying the control interface and the statistics in the system.

III. GEM TEST

To demonstrate the potential of the GEM, some important attributes of GEM are tested, we implemented the following four test cases:

Correctness test: we monitored the incoming and outgoing signals of the GEM to verify correctness of the hardware interface on the FPGA. In addition, we transfer data from the GEM to a client PC using linear values. the GEM sent 1 Giga bytes to PC every time, the client received data and displayed a linear growth, the test result is shown in Fig. 4, there are no errors in the transmission.

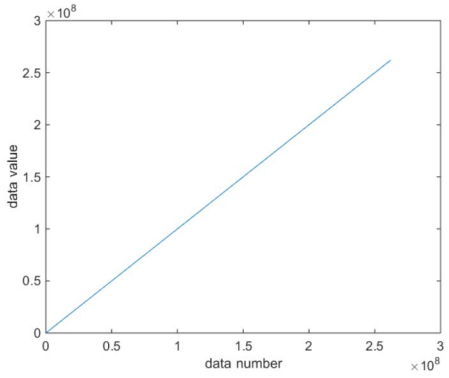

Fig. 4 Linear data correctness test.

Performance test: We also estimated the transfer speed and stability, for this experiment, the GEM was programmed to transmit user data with 1,280 bytes at a user-define frame, as specified in the IEEE STD 802.3 2002 specification[8]. We controlled the generated rate of these data using a counter in FPGA. The received rate increased linearly when we increased the generated rate. Our tests show a transmission rate higher than 900 Mbps and a success rate is 100%.

Long term stability of the GEM is also tested, It runs two and an half hours. Also, the packet loss is tested in real time by embedding a sequence number into each packet sent to the computer. The test result is shown in Fig. 5.

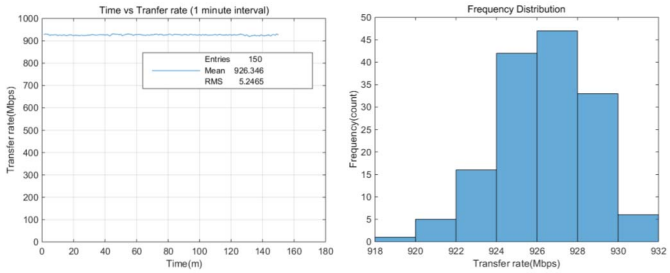

Fig. 5 Transfer speed and stability test. Measure the transfer rate for 150 minutes, sample interval is 1 minute.

The transfer rate is measured for 150 minutes and sample once every minute. The average transfer rate is calculated by the software per minute. From the figure, the average Ethernet transfer rate can reach up 926.3 Mb/s.

BER test: We also performed bit error ratio (BER) measurements on the link implemented with our GEM. More than 10^{12} bits have been transferred continuous and no errors have been observed, corresponding to a 10^{-12} BER.

In these test scenarios show that GEM is reliably transmitted back and forth within a long time, thereby allowing for extensive real world application in our front-end electronics design.

IV. GEM APPLICATION

The GEM has been applied in a dedicated test situation and has been proven to be robust and to meet performance requirements. We present the projects currently using it in pFEB and SG

A. pFEB

A pFEB design based on a ASIC has been developed to read-out pads signals from sTGC dectectors. The second prototype version of this ASIC is called VMM2 chip, which provides the peak amplitude and time with respect to the bunch crossing clock or other trigger signal, in a data driven mode. A VMM2 has 64 channels input, there are four VMM2 chips on each pFEB for sampling 256 channel signal of the sTGC detector. The board can provide Ethernet communication interface and Mini-SAS interface. The architecture of pFEB is illustrated in Fig. 6.

There are two FPGAs on the board for user logics and input/output interface. The Ethernet interface is response for the communication between pFEB and PC. Both the configuration of the VMM2 and digitized readout of the channels peak values are transmitted over Ethernet through MAC (Media Access Control) protocols. The network scheme has been successfully used for testing, and in the next step, we will evaluate the performance of pFEB base on the readout data via Ethernet transmission.

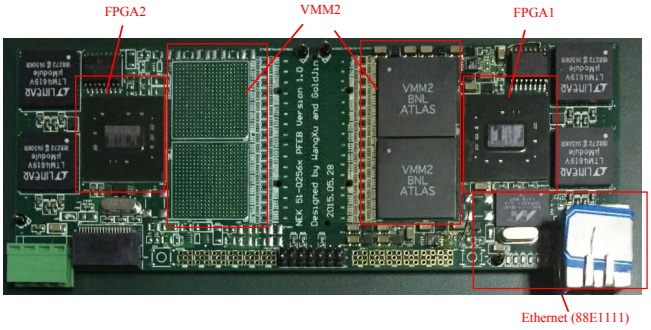

FIG. 6. Module of pFEB for sTGC detector which has 256 channel input, 2 VMMs and 2 FPGAs were assembled on the board, another 2 VMM2 not assembled.

B. SG

The SG concept is based on the test requirements of pFEB or strip FEB (sFEB) which are developing for the future upgrade of the ATLAS NSW Muon detector. It is mainly used to emulate the output of sTGC detector for testing and verifying the FEB electronics and data acquisition system conveniently, checking the performance of FEB. It has been designed into 256 channels and every channel can output a signal for simulating the particles hits the sTGC detector per 25ns. In the process of research and development of FEB, it can test their functions and performances quickly. The specification of SG is below.

- 256 independent charge outputs with both GFZ-30 and Zebra (103mm) connectors. AC coupling
- Configuration via a PC through Ethernet
- Output amplitude depend on output capacitor, for example, 1pf of capacitance vs 2pc.
- Programmable period output of charge pulse, 40MHz Maximum frequency.
- Random charge pulse output in both channel and time
- It can simulate pad, wire and strip signal in the case of real application.
- Charge pulse will be monitored and send back to PC via Ethernet. The data can be displayed on PC screen.

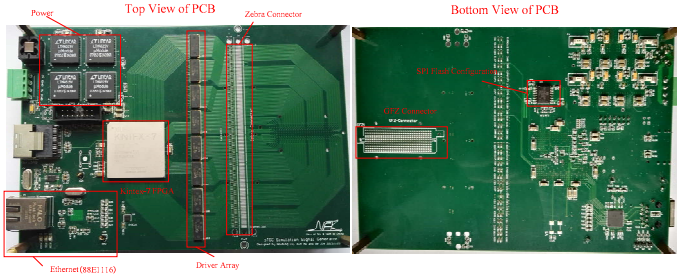

FIG. 7. The photograph of SG. It can be configured into six modes through an Ethernet interface. It can generate test signal for pFEB. The charge signal is delivered into the pFEB through Zebra-256 connector and GFZ-300 connector.

The SG has been developed as shown in Fig. 7. It can provide 6 modes for test application of pFEB and sFEB.

- All channel output. Output uniform pulse for all 256 channel simultaneously
- One channel output. A nominated channel outputs a period pulse.
- Scanning pulse output channel by channel
- Group output. Five adjacent channels output simultaneously
- Group random output. Output five adjacent channels randomly.
- Random signals output. A nominated channel outputs the random pulse.

V. Conclusion

The GEM prototype has been developed. The GEM processes the data with Xilinx FPGA and transfers data to a computer via Ethernet with MAC protocol, which is a technology to realize direct access and transfer of the data in the FIFO of FPGA from the PC. The test show that it can achieve a high speed data transfer and long term stability. Two application based on the GEM have been developed, for the test of the pFEB and SG, the GEM can work properly and give excellent results.

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