Multi-Channel FPGA-Based Data-Acquisition-System for Time-Resolved Single-Photon Counting in Synchrotron Radiation Experiments

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1. Motivation: fundamental and applied science

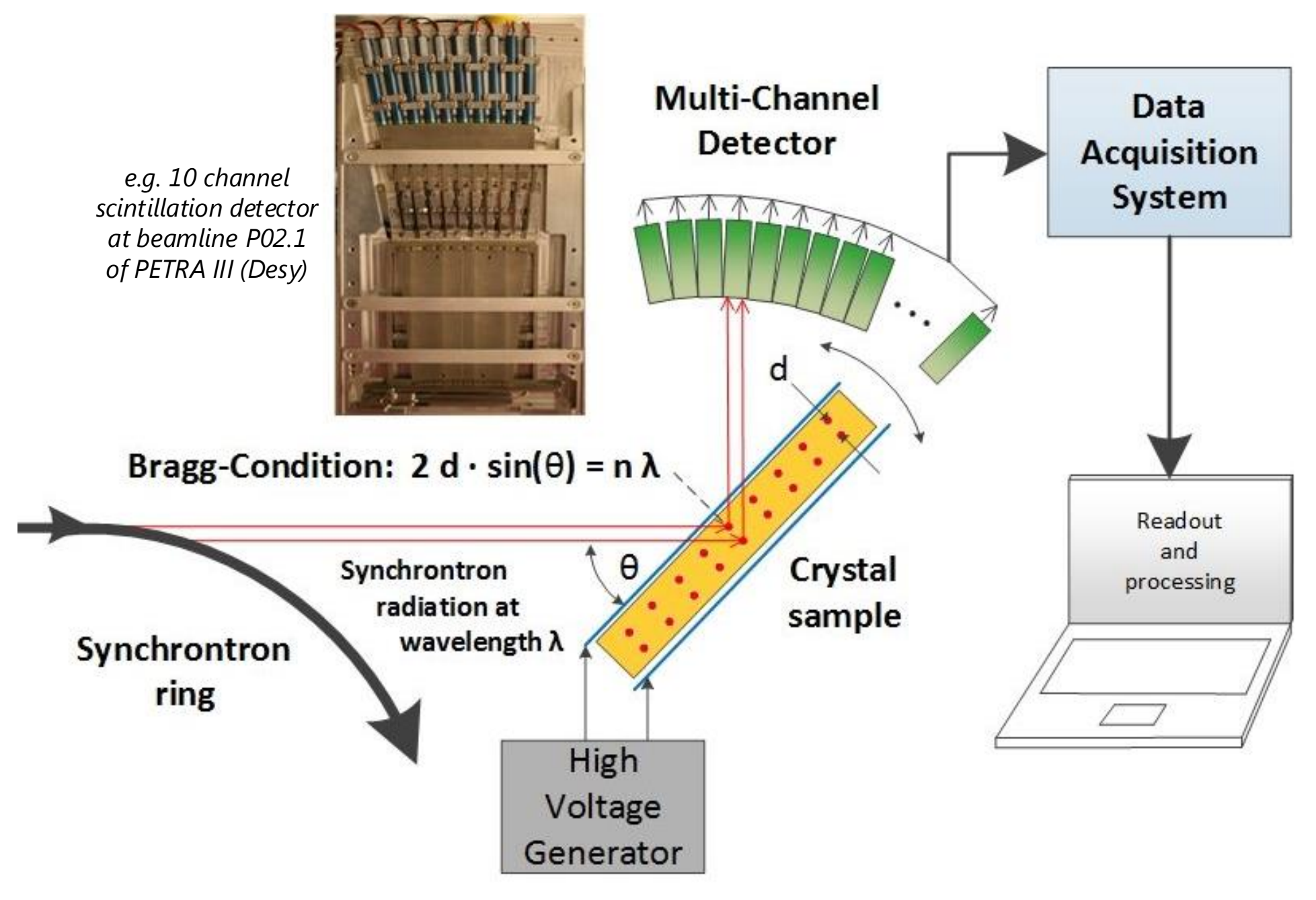

Figure 1: A block diagram of the setup for time-resolved X-ray diffraction experiments.

- ***Structural dynamics of crystals***: the topic of high interest for X-ray crystallography.
- Studied by observing ***Bragg diffraction patterns*** with X-ray or synchrotron radiation under dynamically applied ***external electric field perturbations*** (~Hz to ~MHz); *Figure 1.*
- Different time scales on which crystals react to perturbations connect to different physical mechanisms describing response phenomena:
  - **Change of peak intensity** ↔ *electron and atomic dynamics* with characteristic timescales of **fs** to **ps**.
  - **Intensity re-arrangement between peaks** ↔ *mesoscopic dynamics, e.g. domain wall motion* with characteristic timescales below **ns** to **ms**.
  - **Angular shift of Bragg reflections** ↔ *lattice and domain macroscopic dynamics* with characteristic timescales of **µs** to **ms** and beyond; *Figure 2.*
- Demand on new data acquisition electronics (DAQ systems) suitable for time-resolved measurements of Bragg diffraction patterns with multi-channel point-detectors simultaneously; currently 12 channels.

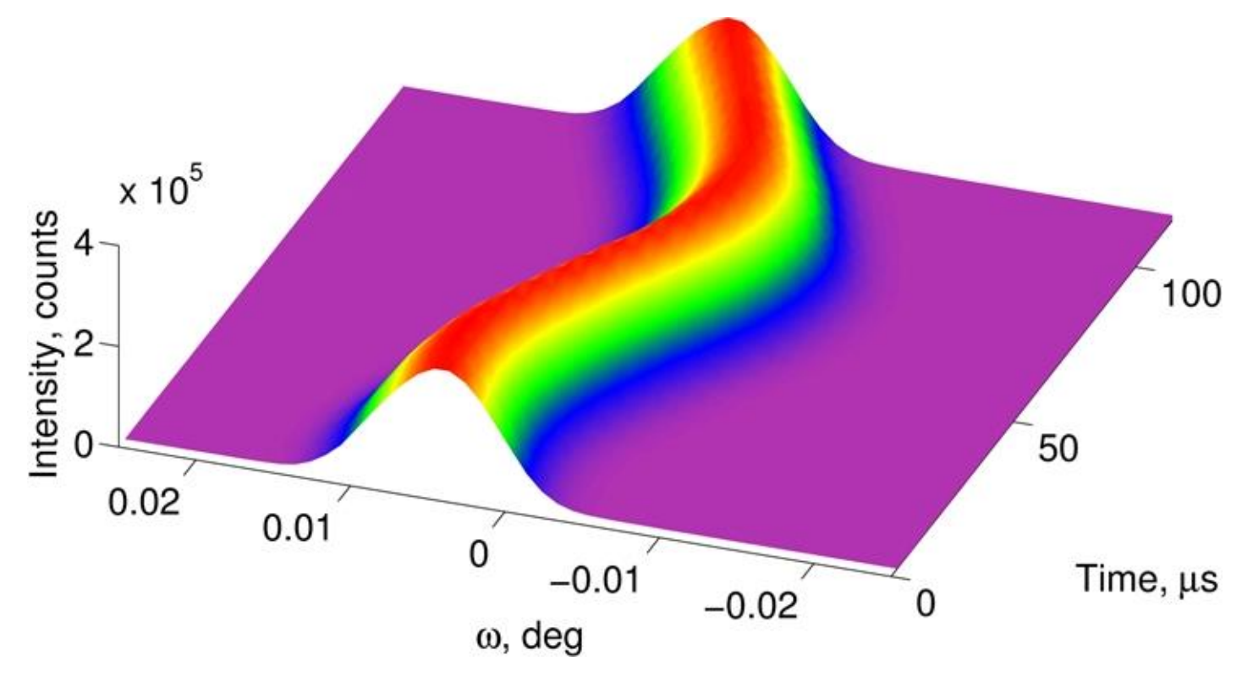

Figure 2: Angular shift of an Bragg reflection in time under applied electric field pulse for the quartz crystal; measured with our single channel DAQ system.

- Our new DAQ system: easily portable between synchrotron facilities and scalable in terms of detector channels.
- Used successfully for our novel time-resolved X-ray diffraction experiments at synchrotron facilities of PETRA III (DESY), BESSY II (Berlin) and ESRF (Grenoble).

2. Operating Principle of our DAQ system

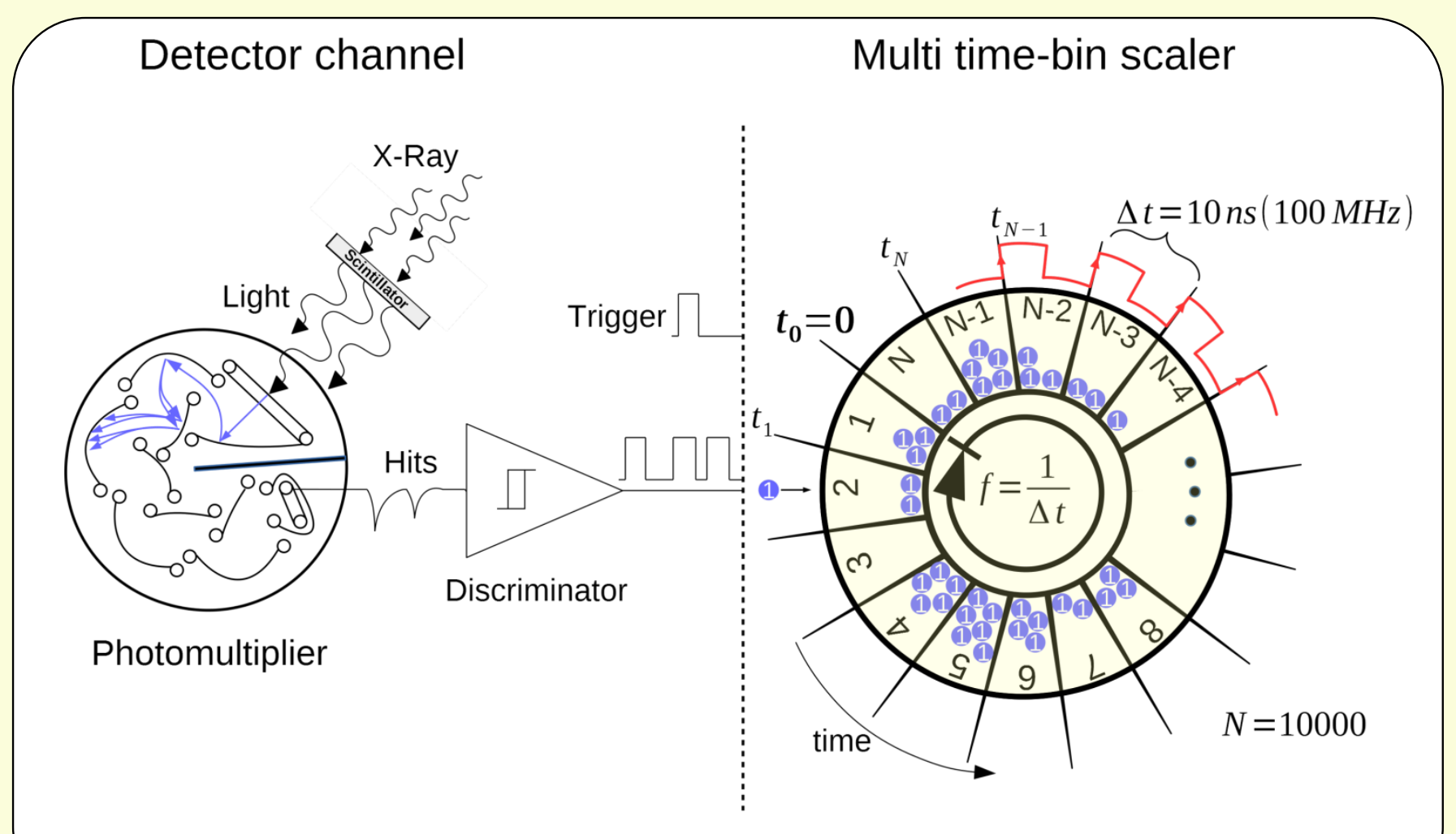

Figure 3: The operating principle of our DAQ system; an intuitive model.

- X-ray diffraction photons converted into light photons by scintillation material.
- Light photons converted into electrical pulses by photo-multiplier. Pulses standardized by a discriminator and applied to the DAQ electronics.

An ***intuitive model*** for one detector channel; *Figure 3*:

- stepwise rotating wheel with time-bin compartments of 10 ns width, moved synchronously by 100 MHz clock.
- 10 000 wheel compartments, each one capable of storing photon hits arriving in a respective time bin of 10 ns.
- Trigger pulse resets time and starts data collection.
- Photon arrival time analysed by the stepping wheel:
  - ❖ hits injected into corresponding time compartments and summed up with counts already gathered.

The ***system*** of 12 parallel working channels.

3. System Architecture

- ➢ Designed in VHDL (hardware description language)
- ➢ Implemented on FPGA (field programmable gate array)
- ➢ Five functional blocks; Figure 4:

- ***Signal Capture***: photon-induced pulses of > 3 ns duration, asynchronously captured and synchronized by 100 MHz clock.
- ***Multi-Channel Scaler (MCS)***: assigns arrival time-bin to captured signals, counts the signals falling in the same time-bin.
- ***Data Storage (RAM)*** for histograms of photon counts (16-bit) versus time-bin index (10 000).
- ***Readout Logic***: supports a Serial-to-USB readout of the RAM by the control computer.

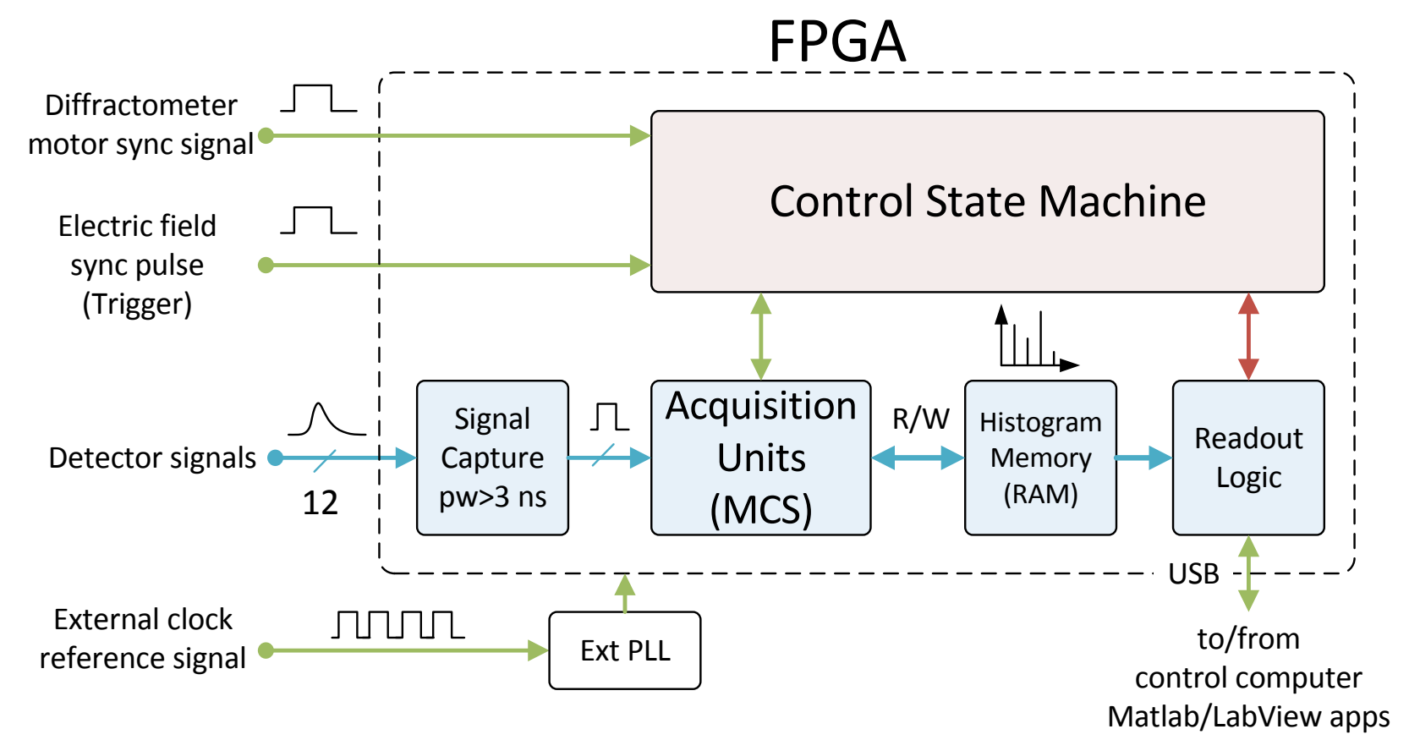

Figure 4: The architecture of our DAQ system.

- **Control State Machine**: coordinates sub-systems, controlled by the Trigger and Diffractometer-Sync signals.
- **Ext PLL** (PLL) for system synchronization with external arbitrary clock sources; not a part of FPGA.

4. Functional design on FPGA

Design features of the ***Multi-Channel Scaler (MCS)*** with 10 ns resolution; *Figure 5*.

- Photon hits captured by fast asynchronous logic, then synchronised with 100 MHz system clock for the timestamping.
- System capable of processing one hit per each clock cycle.
- Counting of photon hits and Read/Write memory access would take several clock cycles per hit.

Therefore

- ➢ buffering of hits for a period of eight clock cycles
- ➢ inside a dedicated 8 x 1 DEMUX register

is utilised.

- Buffered hits are passed to eight parallel ADDERs, where they are summed up with counts previously gathered in the RAM.
- Parallel processing of buffered hits takes five of eight clock cycles available.

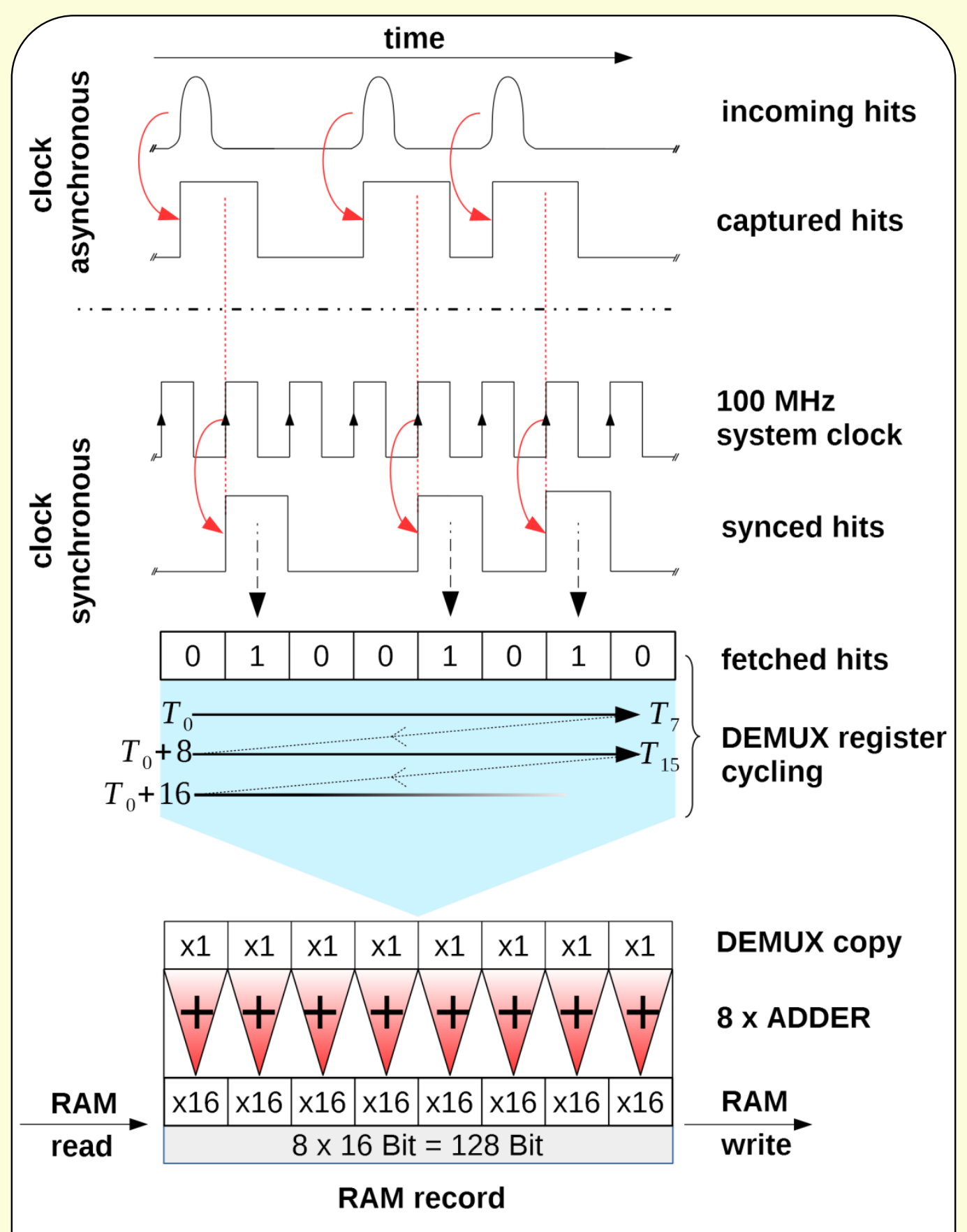

Figure 5: Functional design of our 10ns resolution Multi-Channel Scaler (MCS).

2 ns resolution extension

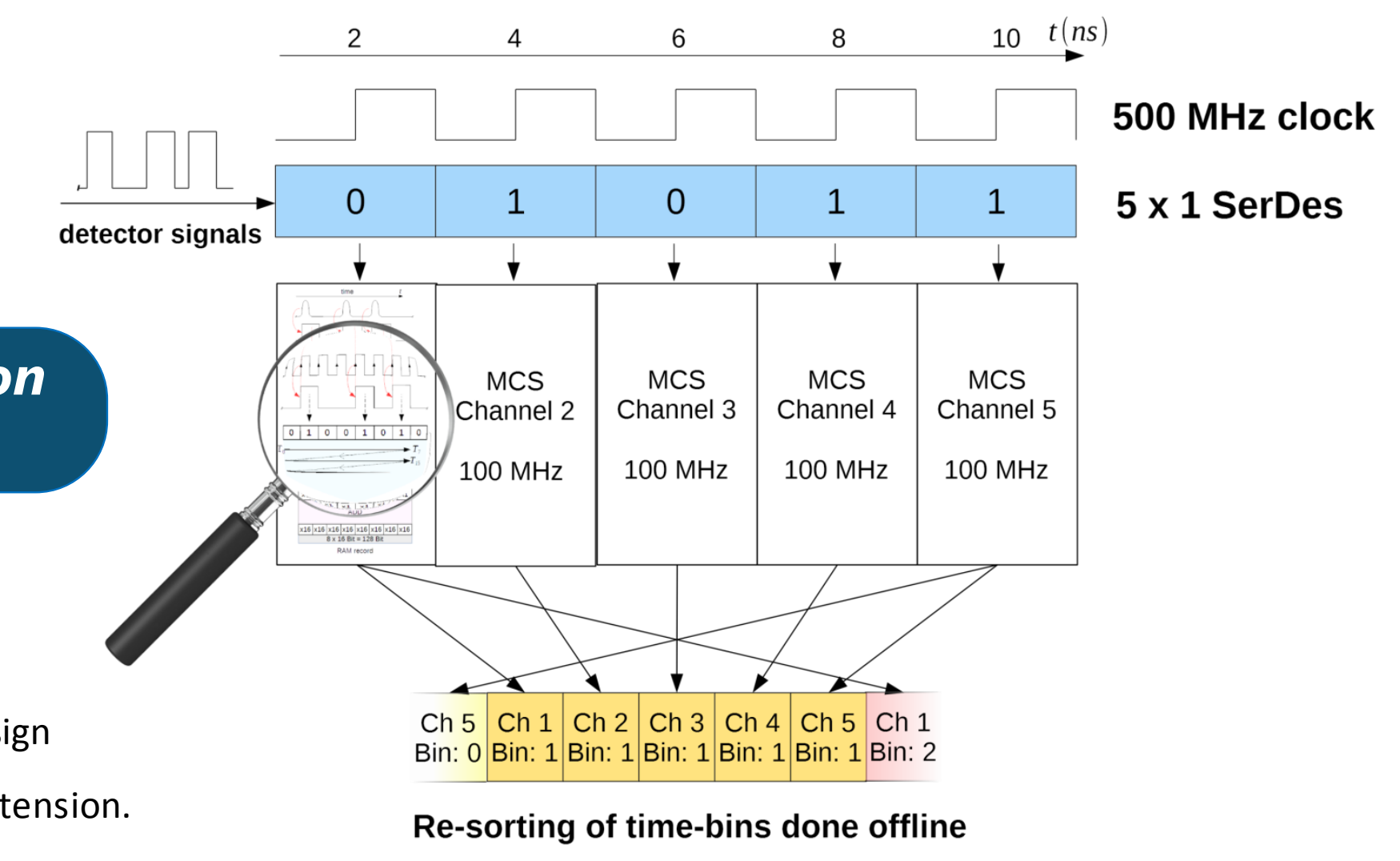

Figure 6: Functional design of the 2 ns resolution extension.

- 1 Gb/s SerDes serial-to-parallel converter used to increase resolution to 2 ns.
- SerDes clock of 500 MHz and register length of five locations; *Figure 6.*
- Incoming photon pulses applied on serial input into SerDes.
- Five parallel SerDes outputs mapped into five MCSs, each of 100 MHz speed.
- Every 10 ns SerDes content copied into *five* parallel running MCSs for hit counting and data storing in RAM.
- Off-line re-sorting of time-bins to a single data stream.

5. Hardware implementation

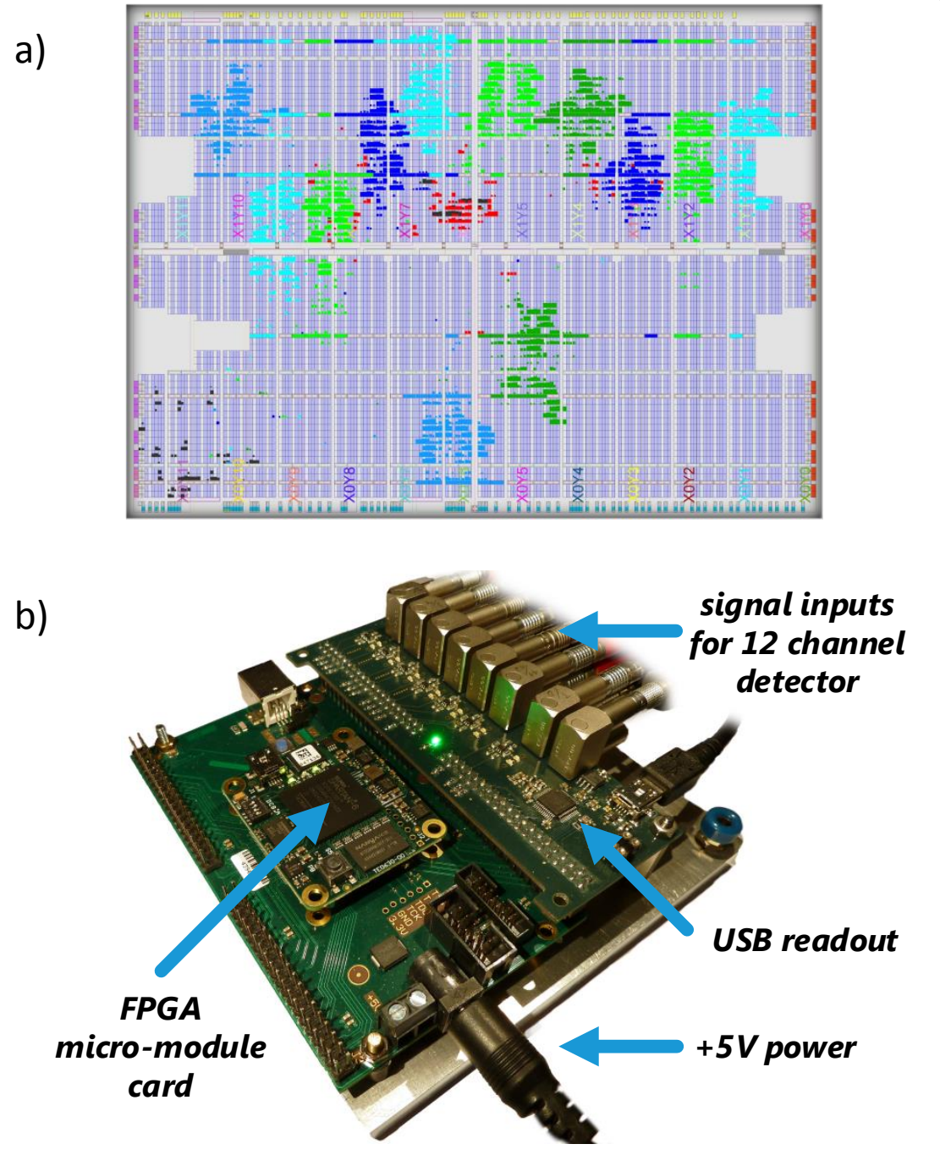

Figure 7: a) The FPGA floor plan, b) the hardware, with 12 independent channels implemented.

Floor plan:

- VHDL design implemented on Xilinx®
  Spartan-6 LX150 FPGA chipset.
- Containing 12 independent channels; *Figure 7 a*.
- **37 %** of configurable logic block (CLB) and
- **53 %** of block RAM resources used.

Hardware:

- FPGA micro-module card, type TE0600 and signal fan-out card; both *Trenz Electronic* products; *Figure 7 b.*
- Home-made daughter card for I/O signals and Serial-to-USB data transmission chipset.

6. Experimental results

➢ 10 ns resolution example from PETRA III:
- 10-channel MAD-detector installed at the Beamline P02.1.
- Our DAQ system of **10 ns resolution**.
- Powder ceramics sample, exited by 10 kHz cycles of a rectangular electric field, probed by the X-ray beam, diffraction profiles obtained.
- Overall intensity of three diffraction peaks collected by three detector channels with quarter millidegree angular resolution; *Figure 8 (left).*
- Time dependence of diffraction profiles measured on µs scale with 10 ns resolution; *Figure 8 (right)*.

➢ 2 ns resolution example from BESSY II:
- A fast single-point detector.
- Our DAQ system of **2 ns resolution** extension.
- Measurement of X-ray multi-bunch time structure with 2 ns bunch separation; *Figure 9.*

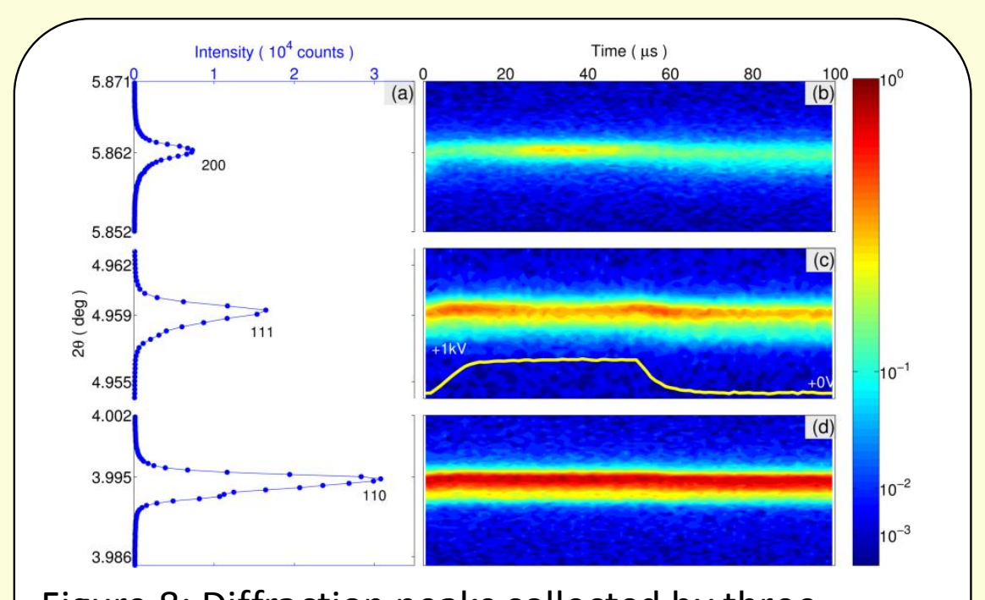

Figure 8: Diffraction peaks collected by three detector channels with 10 ns resolution (PETRA III).

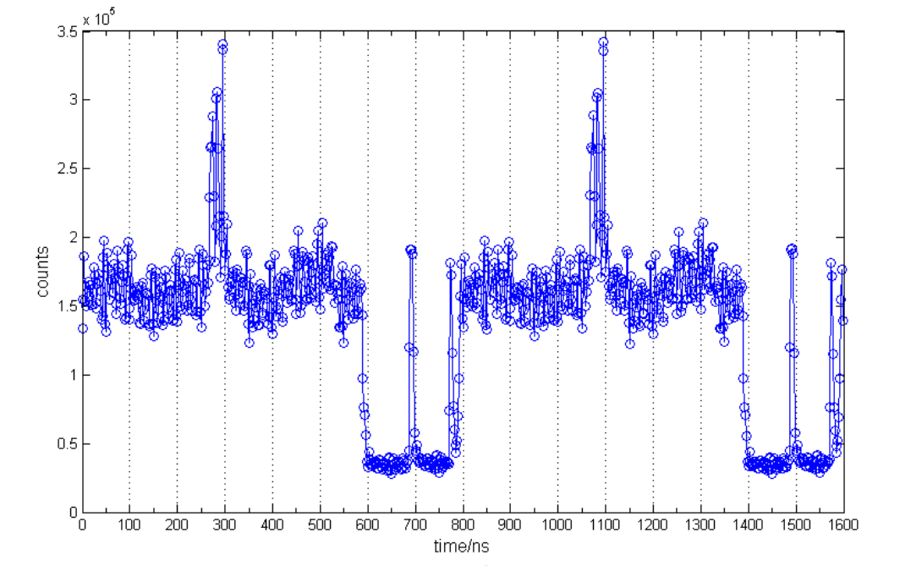

Figure 9: Measurement of X-ray multi-bunch time structure with 2 ns resolution (BESSY II).

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