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Prototype for Low-cost FPGA TDC with High Precision and Density

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Time measurement is indispensable for particle identification in high energy experiments, especially in time-of-flight (TOF) system. An excellent precision of TDC are beneficial to particle identification, and a low dead time facilitates to adapt the high event rate environment of the experiments. TDC implemented in Field Programmable Gate Array (FPGA) has been developed for years and has obtained superior specifications that are enough to meet the requirement. But in an experiment with over ten thousand channels like the Compressed Baryonic Matter (CBM) one, trade-off must be weighed between the performance and cost. Furthermore, massive channels with high event rate of the experiment result in extra-high time measurement data rate, which is a big challenge for real-time data transmission. Thus, with the ongoing upgrade of high energy physical experiment, it has great significance to develop a TDC prototype that accommodates high data rate with satisfying precision and cost.In this paper, a prototype containing 320 time measurement channels with 15 ps precision and a data transmission link with up to 10 Gbps rate is presented. The prototype is designed as a sandwich structure, which mainly consists of a TOT Feeding Board (TFB), a TDC Readout Motherboard (TRM) and ten in-between 32-channel TDCs plugged in foregoing two boards perpendicularly. The TDC is implemented in Xilinx's low-end Artix-7 FPGA to furthest reduce the cost, and the principle of time measurement is based on a coarse time counter combining with the dedicated high-speed carry chain for fine time measurement. The counter provides 4 ns coarse resolution in 250 MHz system clock, and the carry chain is utilized for time interpolation within a system clock period. Its precision of 15 ps is enough to satisfy most experiment requirement including CBM TOF. The TDC also supports time-over-threshold (TOT) measurement, and the precision of pulse width measurement is better than 30 ps. To accommodate the 100 ˜ 300 kHz single channel event rate in CBM TOF, a gigabit transceiver called GTP integrated in FPGA is used in TDC. Thus each TDC is able to transmit 32 channels'data at more than 1 Gbps rate. TRM in our prototype gathers the 10 TDCs'time measurement data and transmit it to back-end readout crate via optic fibers. The data rate of TRM is up to 10 Gbps by applying gigabit transceivers called GTXs integrated in Kintex-7 FPGA.

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