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Multichannel DAQ IC with zero deadtime and extended input range for current pulse sensors

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This work presents a multichannel IC which is able to process and digitize simultaneous current pulses in every input channel with no deadtime. The analog to digital conversion is performed in two steps: 6 MSBs are quantized by the charge pulse system (CPS) and 8 LSBs are obtained from a later ADC for a total of 14 ENOB at the output.

A wave shaper is needed to distribute the input current more uniformly over the integration period and to reduce the current pulse rising slope. A configurable CR-RC^2 structure is used to implement this block.

The CPS can process bipolar input current. The core of the CPS is an integrator controlled by two comparators. When the output voltage exceeds any of two fixed thresholds, an auxiliary capacitor is connected and charge pumping to the integration capacitor is produced, keeping its value inside a given range. As a consequence the CPS behaves as an asynchronous and self-regulating system. The integrator can work in continuous time, with no reset operation of the integration capacitor. Moreover the dynamic range of the input current is increased by over two decades and at least 20 dB SNR improvement can be obtained.

The number of pulses produced by the charge pump is stored in an asynchronous counter and represents the MSBs. A maximum of 100 charge pulses can be achieved due to settling time limitations for an integration period of 1us, thus obtaining 6,6 MSBs. The remaining voltage is the difference between the integrator outputs at the beginning and at the end of the integration period which are quantized later by an ADC.

The high precision trigger system detects the start of the input pulse current event and activates storage of the integrator output voltage in a capacitor based memory cell (MC). Once the integration is finished, the output voltage is stored again in a second MC. An 8 bits SAR type ADC converts both values without deadtime taking advantage of the design pipeline structure.

Finally the last stage is composed of digital logic which has three main functions. First one is to subtract two ADC output values. The result corresponds to the LSBs of the final digital code. This operation allows avoiding baseline shift effects and also cancels low frequency noise components such as flicker noise. The second function is to sum both MSBs and LSBs in order to obtain the 14 effective bits at the IC output. Digital logic also has to synchronize and control the ADC and MCs.

The IC is designed for sensors with fast pulse current responses such as SiPM. The CPS extended input range can take advantage of high gain sensors thus improving overall SNR of the detector. Energy resolution dependent applications such as PET might benefit from this novel DAQ architecture.

The extracted layout simulations of the chip will be presented for the conference record.

Authors: MAZUR, Dmytro (UPV); MONZO, Jose M. (Universidad Politécnica de Valencia); GADEA, Rafael (U); ALIAGA, Ramon J. (Instituto de Fisica Corpuscular); HERRERO-BOSCH, Vicente (Universidad Politécnica de Valencia)

Presenter: MAZUR, Dmytro (UPV)

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