Multichannel DAQ IC with Zero Deadtime and Extended Input Range for Current Pulse Sensors

P220

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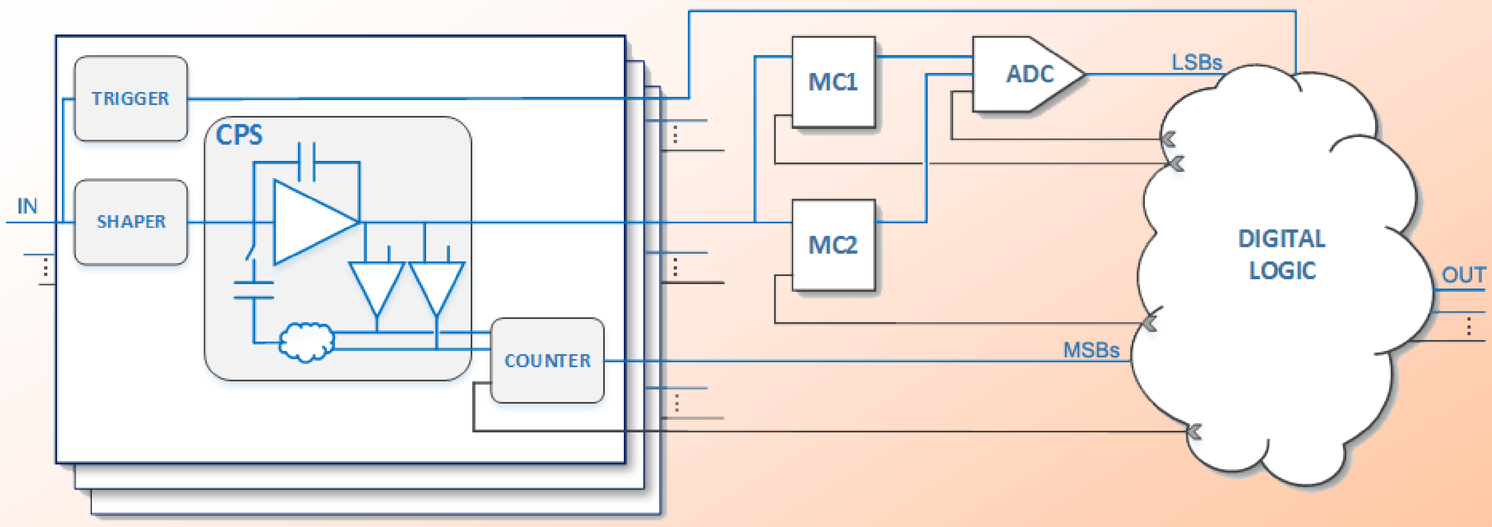
IC ARCHITECTURE

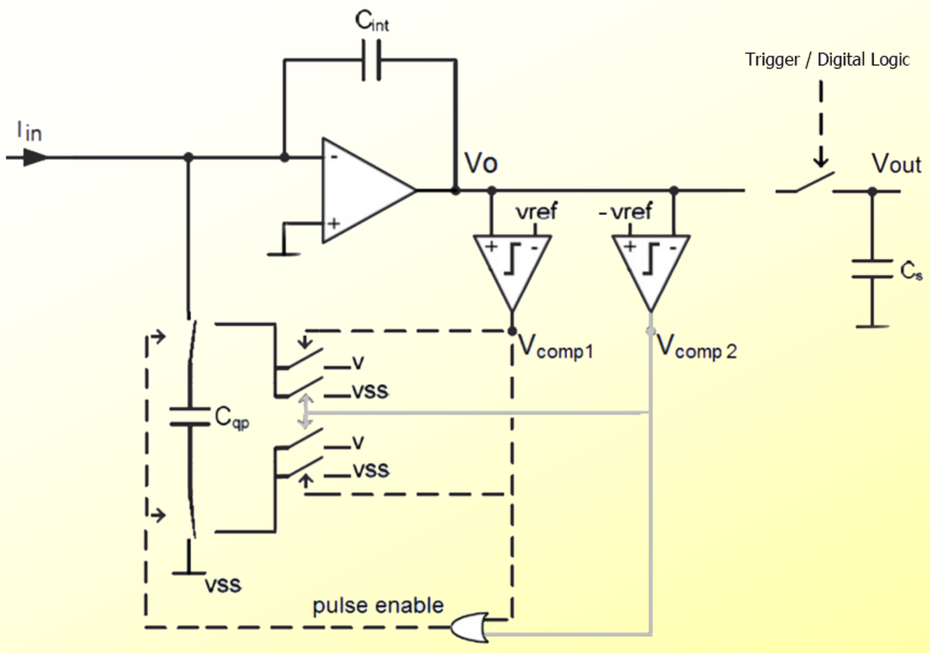


- IC designed for sensors with fast pulse current responses
- The CPS extends the input current dynamic range
- No deadtime due to pipeline architecture
- The analog to digital conversion is performed in two steps: 6 MSBs are quantized by the CPS and 8 LSBs are obtained from a later ADC for a total of 14 ENOB at the output

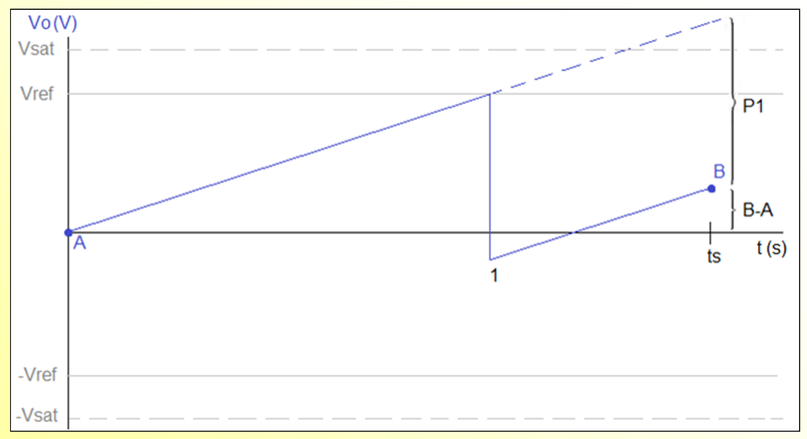
- **Trigger** (1 per channel)
  - detects the input current pulse and initiates the integration period
- **Shaper** (1 per channel)
  - distributes the input pulse current more uniformly over the integration period
- **Charge Pulse System** (**CPS,** 1 per channel)
  - integrates the input current
  - self-regulates avoiding the saturation by injecting charge pulses and shifting the integrator output voltage
- **Two capacitor-based Memory Cells** (**MC,** 2 storage capacitors per channel)
  - store the integrator output voltage at the beginning (MC1) and at the end (MC2) of the integration period
- **ADC** (1 per 8 channels)
  - converts alternating between MC1 and MC2 samples
- **Asynchronous counter** (1 per channel)
  - counts CPS pulses and quantizes it as MSBs
- **Digital control logic**
  - quantizes the LSBs as the difference between two consecutive ADC conversions
  - sum of both MSBs and LSBs
  - synchronizes and controls the ADC and MCs

PRINCIPLE OF CPS OPERATION

CPS: asynchronous self-regulating Charge Pulse System



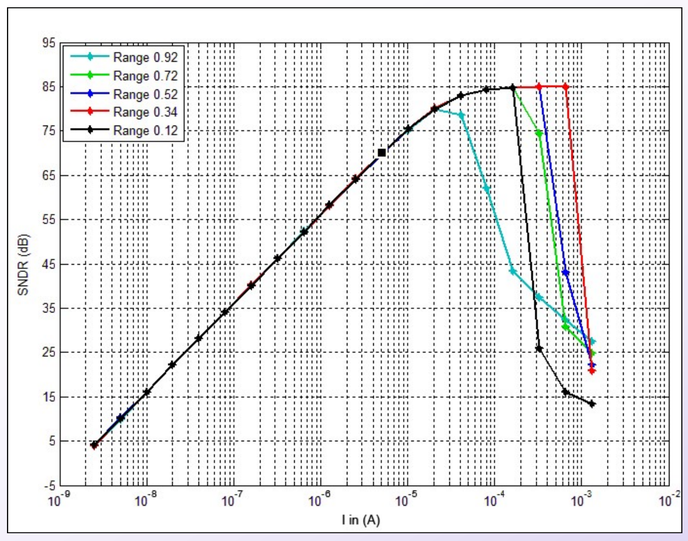
- The CPS can process bipolar input currents.
- The core of the CPS is an integrator controlled by two comparators. When the output voltage (*Vo*) exceeds any of two fixed thresholds (*vref* / - *vref*), an auxiliary capacitor (*Cqp*) gets precharged and is connected to the integrator. Charge pumping to the integration capacitor (*Cint*) is produced.
- The CPS behaves as an asynchronous self-regulating front-end and the integrator can work in continuous time, with no reset operation of *Cint*.



The plot shows the integrator output voltage for negative constant input current. The dashed line represents the output front-end voltage without CPS, which results in saturation for a given input current. By injecting the negative charge pulse (P1), saturation is avoided, thus extending the dynamic range of the input current.

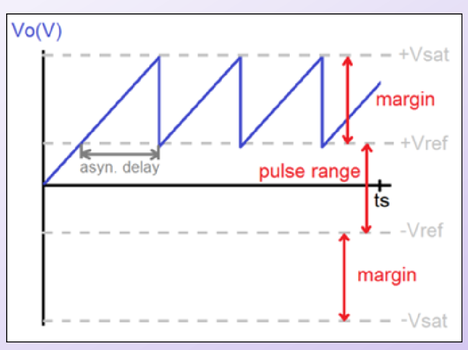
The ADC converts the *Vo* signal two times (points A and B) per integration period.

FIRST RESULTS



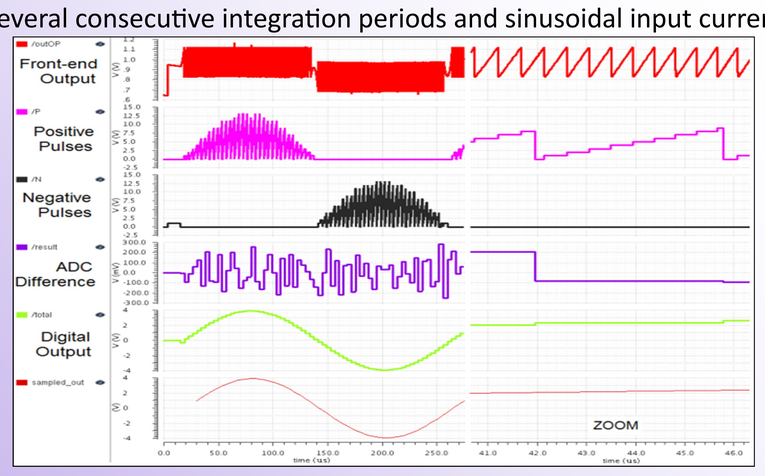
- The ASIC is currently at the schematic stage, using 0,18 µm CMOS technology (AMSC18)
- A 85.5 dB SNR is obtained for a 0,5 mA rms input pulse which corresponds to 14.2 ENOB
- The circuit can process pulse currents with peak values up to 2,5 mA without saturation

There is an optimal pulse height (1/3 of total ±*Vsat* ADC range), which increases the allowed range for the input current. The margins are used to allow integration of the current during the delay time from the current overflow to charge pulse activation.



Limitation of maximum input current:
The large *Iin* produces a large *Vo* increment almost equivalent to the charge pulse size during the pulse activation delay. The comparator is activated at the beginning of the asynchronous delay and the charge pulse is produced at the end of it.

Several consecutive integration periods and sinusoidal input current



One integration period and pulse type input current