Multichannel DAQ IC with Zero Deadtime and Extended Input Range for Current Pulse Sensors

D. Mazur, V. Herrero Bosch, R. J. Aliaga, J. M. Monzó Ferrer, R. Gadea Gironés, R. J. Colom Palero

***Abstract*-- This work presents a multichannel IC architecture which is able to process and digitize simultaneous current pulses in every input channel with no deadtime. The analog to digital conversion is performed in two steps: 6 MSBs are quantized by the Charge Pulse System (CPS) and 8 LSBs are obtained from a later ADC for a total of 14 ENOB at the output.**

An IC designed for sensors with fast pulse current responses is currently under development. The CPS extended input range can take advantage of high gain sensors thus improving overall SNR of the detector. Energy resolution dependent applications such as PET might benefit from this novel DAQ architecture.

***Index Terms*—charge pulse, integration front-end, zero deadtime, extended dynamic range, self-regulating system.**

I. Introduction

There is a trend to employ Silicon Photomultipliers (SiPM) as sensors for PET applications due to their large gain and the time resolution lower than 100ps [1]. The current yielded by this type of sensors can be quite large and taking advantage of this feature may lead to improved energy resolution. The integrator type front-end [2] can manage the sensor current and convert it to voltage inside the operating range limited by the power supply, where the maximum resolution is determined by the frontend noise floor. Some front-ends even use simpler architecture, such as Time over Threshold (ToT) [3] which is an approximation of integration but with less resolution.

The presented architecture in this work is being designed as 32 channel ASIC for current conditioning of SiPM sensors. The approach followed in this work is to perform the conversion in several steps taking advantage of the increased input front-end dynamic range for large output SiPM current. The proposed front-end is compatible with time stamp generation for temporal processing of detected events.

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II. Circuit Architecture

Figure 1 shows the blocks used in the IC implementation:

- Trigger (1 per channel)
- Shaper (1 per channel)
- Charge Pulse System (CPS, 1 per channel)
- Two capacitor-based Memory Cells (MC, 2 storage capacitors per channel)
- ADC (1 per 8 channels)
- Asynchronous counter (1 per channel)
- Digital control logic

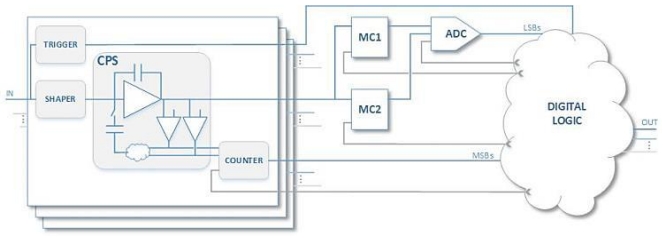

Fig. 1. Block diagram of the IC implementation.

A. Shaper

A shaper circuit is needed to distribute the input current more uniformly over the integration period and to reduce the current pulse rising slope. A configurable CR-RC² structure is used to implement this block [4].

B. Charge Pulse System

Figure 2 represents the CPS structure. The CPS can process bipolar input currents. The core of the CPS is an integrator controlled by two comparators. When the output voltage (V_o) exceeds any of two fixed thresholds (V_{ref} / $-V_{ref}$), an auxiliary capacitor (C_{qp}) gets precharged and is connected to the integrator. Charge pumping to the integration capacitor (C_{int}) is produced: if V_o exceeds the upper limit (V_{ref}), a downward voltage pulse immediately occurs, or an upward pulse if the lower limit is reached ($-V_{ref}$), keeping V_o within the operating range.

Hence the CPS behaves as an asynchronous and self-regulating front-end [5] and the integrator can work in continuous time, with no reset operation of C_{int}. Moreover the dynamic range of the input current is increased by over two decades so that a SNR improvement of at least 20 dB can be obtained.

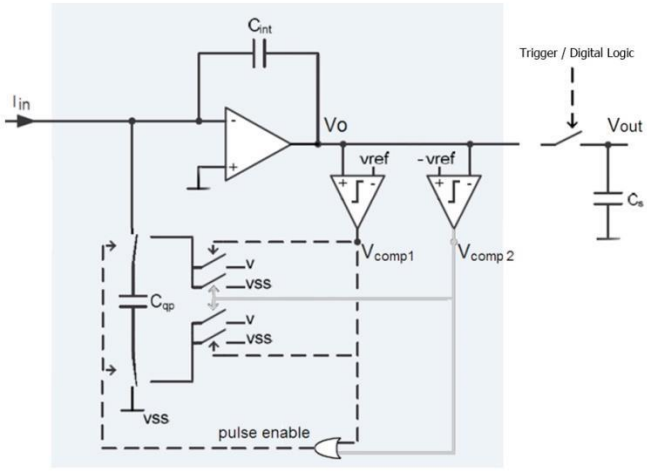

Fig. 2. CPS structure: integrator, two comparators and charge pulse system.

Figure 3 shows a plot of the integrator output voltage for negative constant input current. The dashed line represents the output front-end voltage without CPS, which results in saturation for a given input current. By injecting the negative charge pulse (P1), saturation is avoided, thus extending the dynamic range of the input current.

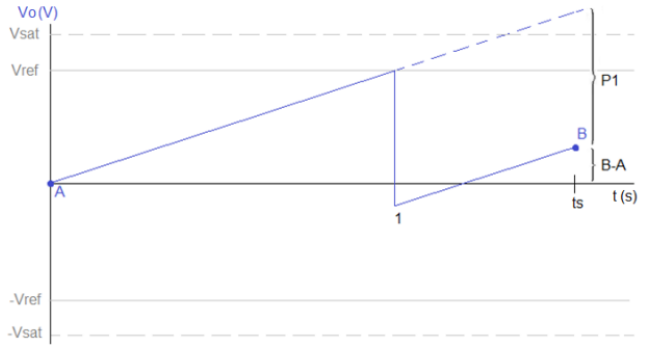

Fig. 3. Integrator output voltage for negative constant input current.

There are significant advantages in asynchronous front-end for small and large input currents:

- When I_{in} is small the output integrator ramp has smooth slope and it takes more time to reach the V_{ref} level, therefore it can occur that no pulse is produced in some integration periods, with the ADC converting the shifted integration signal. Thanks to it there is no noise due to the charge pulses (or C_{int} reset which is performed in other types of front-ends).
- For large I_{in} saturation can be avoided by injecting many consecutive pulses. Saturation only occurs when the V_o increment from V_{ref} (comparison voltage to enable charge pulse) to V_{sat} is faster than the timing delay during the timing delay of pulse enable. Of course the pulse enable delay can be minimized using higher bandwidth which might require higher power consumption. This establishes the limitation on maximum input current.

Figure 4 shows how the large I_{in} produces a large V_o increment almost equivalent to the charge pulse size during the pulse activation delay. The comparator is activated at the beginning of the asynchronous delay and the charge pulse is produced at the end of it.

Since there is no saturation the SNR increases due to larger input signal.

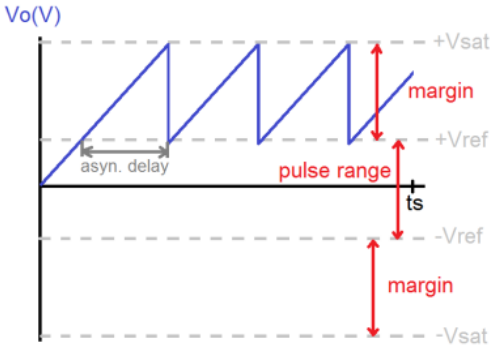

Fig. 4. Front-end behavior for large constant input currents.

Figure 5 shows a comparison between asynchronous front-ends with different output ranges. The charge pulse height is close to the range in every case. It can be seen that there is an optimal pulse, which increases the allowed range for the input current. The optimal pulse occurs when the separation between comparison levels (pulse range between $+V_{ref}$ and $-V_{ref}$, see Figure 4) is 1/3 of total ADC range ($\pm V_{sat}$), allowing 1/3 of upper margin (between $+V_{ref}$ and $+V_{sat}$) and 1/3 of lower margin. The margins are used to allow integration of the current during the delay time from the current overflow to charge pulse activation without reaching V_{sat}.

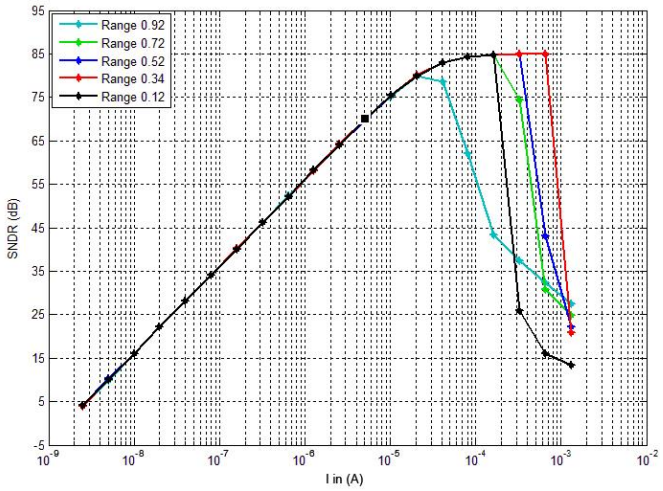

Fig. 5. SNR versus Input current for different pulse ranges.

C. Counter, ADC, Trigger and MCs functions

The amount of pulses V_{comp1} and V_{comp2} (Figure 2) which activate the charge pump is stored in an asynchronous counter. A coarse ADC code is obtained by multiplying the number of pulses by the pulse height previously quantified with the ADC. Using 0,18 µm CMOS technology (AMSC18) a maximum of 100 charge pulses can be achieved for 1µs of integration period due to settling time, thus obtaining 6,6

MSBs. The remaining voltage (fine code) is the difference between the integrator outputs at the beginning and at the end of the integration period which are quantized later by an ADC.

A high precision trigger system detects the start of the input pulse current event and activates storage of the integrator output voltage in a capacitor based memory cell (MC). Once the integration is finished, the output voltage is stored again in a second MC. An 8 bits SAR type ADC converts both values without deadtime taking advantage of the design pipeline structure. In Figure 3 the ADC converts the V_o signal two times (points A and B) per integration period (*ts*).

D. Digital control logic

Finally the last stage is composed of digital logic which has three main functions:

- Subtraction of two consecutive ADC output values (Figure 3: B - A). The result corresponds to the LSBs of the final digital code. This operation allows compensating baseline shift effects (offset) and also cancels low frequency noise components such as flicker noise.
- Sum of both MSBs and LSBs in order to obtain the 14 effective bits at the IC output.
- Synchronization and control of the ADC and MCs.

III. Simulation Results

The ASIC is currently at the schematic stage, using 0,18 µm CMOS technology (AMSC18). The whole analog signal processing chain has been simulated at the transistor level and high-level models have been used for digital circuitry.

A 85.5 dB SNR is obtained for a 0,5 mA rms input pulse which corresponds to 14.2 ENOB. The circuit can process pulse currents with peak values up to 2,5 mA without saturation.

Figure 6 represents IC waveforms for several consecutive integration periods, simulated in Cadence with sinusoidal input current.

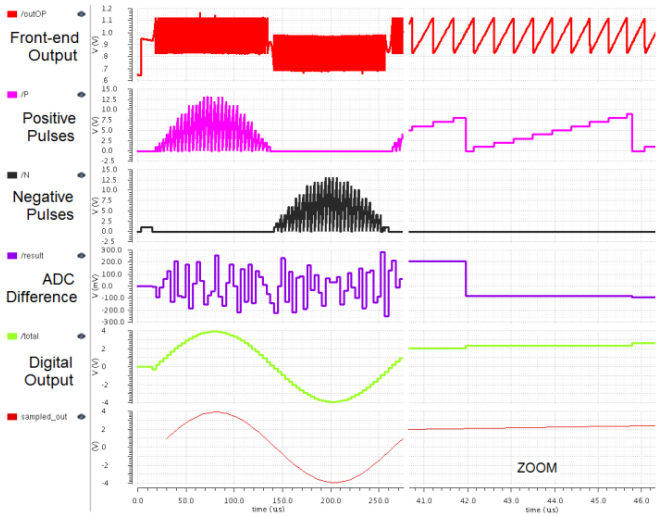

Fig. 6. IC waveforms for several consecutive integration periods and sinusoidal input current.

Figure 7 shows IC wave forms for one integration period. The input current is pulse type. The algebraic sum of pulses and ADC voltage gives the total quantized voltage by front-end. In figure 7 the dynamic range is extended from 1 to 4,69 V.

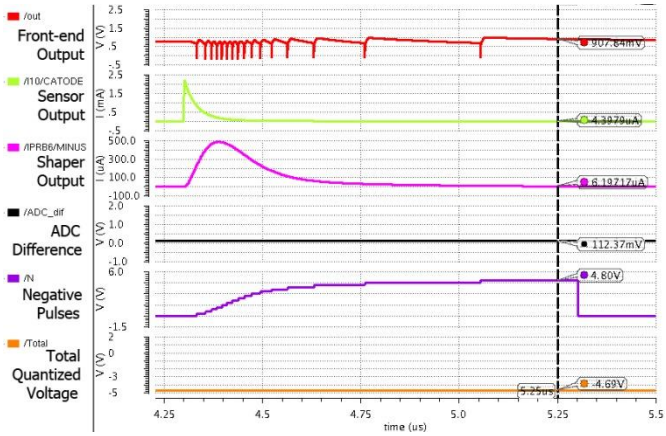

Fig. 7. IC wave forms for one integration period and pulse type input current.

IV. Conclusions

A multichannel IC is proposed for current pulse sensors. A new front-end architecture with higher precision is presented as an alternative to ToT. The main important characteristics of this front-end are: extended input current range, zero deadtime, self-regulation and reduced noise for small input currents.

The design is currently at the schematic stage and intended to be set to foundry by October 2016.

V. References

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