A DAQ Prototype for the ATLAS small-strip Thin Gap Chamber Phase-I Trigger Upgrade

Kun Hu, Houbing Lu, Xu Wang, Feng Li, Xinxin Wang, Tianru Geng, Hang Yang, Liang Han, and Ge Jin

***Abstract*–we will present a DAQ prototype designed for the ATLAS small-strip Thin Gap Chamber (sTGC) Phase-I trigger upgrade. The prototype includes two VMM2 chips developed to read out the signals of the sTGC, a Xilinx Kintex-7 FPGA used for the VMM2 configuration and the events storage, and a Gigabit Ethernet Transceiver (GET) working at the physical layer. The features of the DAQ prototype are described in detail.**

I. Introduction

ATLAS [1], [2] is one of four experiments that is located at the Large Hadron Collider (LHC) now being constructed at CERN, Geneva, Switzerland. The ATLAS detector accepts the events from the proton–proton collision at a rate of 40 MHz. At high luminosity, the performance of the muon tracking chambers, both in terms of efficiency and resolution, degrades with the increase of the background rate, especially in the end-cap region. Moreover, the low energy protons, generated in the magnet materials between the small wheel (SW) and the end-cap muon detector (EM), hits the end-cap trigger chambers, thus producing fake triggers. In order to cope with these problems, it is proposed by ATLAS collaboration to replace the current muon SW with the 'new small wheel' (NSW). The thin gap chamber (TGC) technology, developed in 1983 [3], is an important part of the SW. The small-strip TGC (sTGC) in which the strip pitch is much smaller than that of the current ATLAS TGC will be applied for the NSW upgrade.

The VMM [4] chip, is able to read out both positive and negative polarity signals for each channel. The current version, VMM2 chip, consists of 64 linear front-end channels. Each channel integrates a Charge Sensitive Amplifier (CSA), a shaper, a stable band-gap referenced baseline, several ADCs and other functions. For an input event rate of 40 MHz, the events are continuously read out by the FPGA with a token clock. Therefore, the high speed data transfer interface is required to send out the events from the sTGC.

In this paper, we will introduce a DAQ prototype based on a high speed gigabit Ethernet interface. The prototype includes two VMM2 chips, a Xilinx Kintex-7 FPGA, and a physical layer Gigabit Ethernet Transceiver (GET). Additionally, the DAQ integrates a high transfer speed mini-SAS interface. The Graphical User Interface (GUI) is written based on Qt application platform, achieving the initialization and control of the DAQ prototype.

Manuscript received May 29, 2016. This work was supported by the National Natural Science Foundation of China under Grants 11461141010 and 11375179, and in part by "the Fundamental Research Funds for the Central Universities" under Grant No. WK2360000005.

Kun Hu, Houbing Lu, Xu Wang, Feng Li, Xinxin Wang, Tianru Geng, Hang Yang, Liang Han, and Ge Jin are with State Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China, Hefei, Anhui 230026, P.R. of China (phone: +86-551-63606495; e-mail: khu@ustc.edu.cn, luhb@mail.ustc.edu.cn, wangxu1@mail.ustc.edu.cn, phonelee@ustc.edu.cn, wxx10@mail.ustc.edu.cn, gudujian@mail.ustc.edu.cn, lanejay@mail.ustc.edu.cn, hanl@ustc.edu.cn, goldjin@ustc.edu.cn).

II. The Prototype Architecture

A. Hardware

The schematic block diagram of the DAQ prototype is illustrated in Fig. 1. The core of the prototype is based on a Kintex-7 FPGA, which is configured by a Serial Peripheral Interface (SPI) flash. Two VMM2s, which are interconnected using a daisy chain, are used to read out the signals from the sTGC detector. The mini-SAS connector is designed to receive the external trigger and the 40MHz synchronized clock. The external trigger emerges from a coincidence of two scintillation detectors over and below the sTGC detector, used for sTGC efficiency test in the future. The 88E1111 Gigabit Ethernet Transceiver is a physical layer device for 1000BASE-T, 100BASE-TX, and 10BASE-T application. In our design, the GET is configured as the Gigabit Media Independent Interface (GMII). The RJ45 port is used for connection between the hardware and a computer.

B. Signal Flow in FPG

The block diagram of the signal flow in the FPGA is shown in the middle of Fig. 1. The Ethernet core, generated via the Core Generator of the Xilinx ISE software, is embedded in the FPGA. The Ethernet interface is implemented in Media Access Control (MAC) layer, which is a sub-layer of the data link layer. The Ethernet interface accepts the user-defined commands and VMM2 configuration bits. The different commands can be derived from the command decoder. At initialization, all the FIFOs and status registers are reset. Then, a VMM2 configuration command arrives. The VMM2 configuration module is implemented via a state machine After the configuration, the VMM2 data (*data0*, *data1*) will output when one of VMM2 channels perceives a charge signal. Once sending a user-defined *data upload* command, events from two VMM2s are stored in an internal FIFO. Then these events are sent back to a computer.

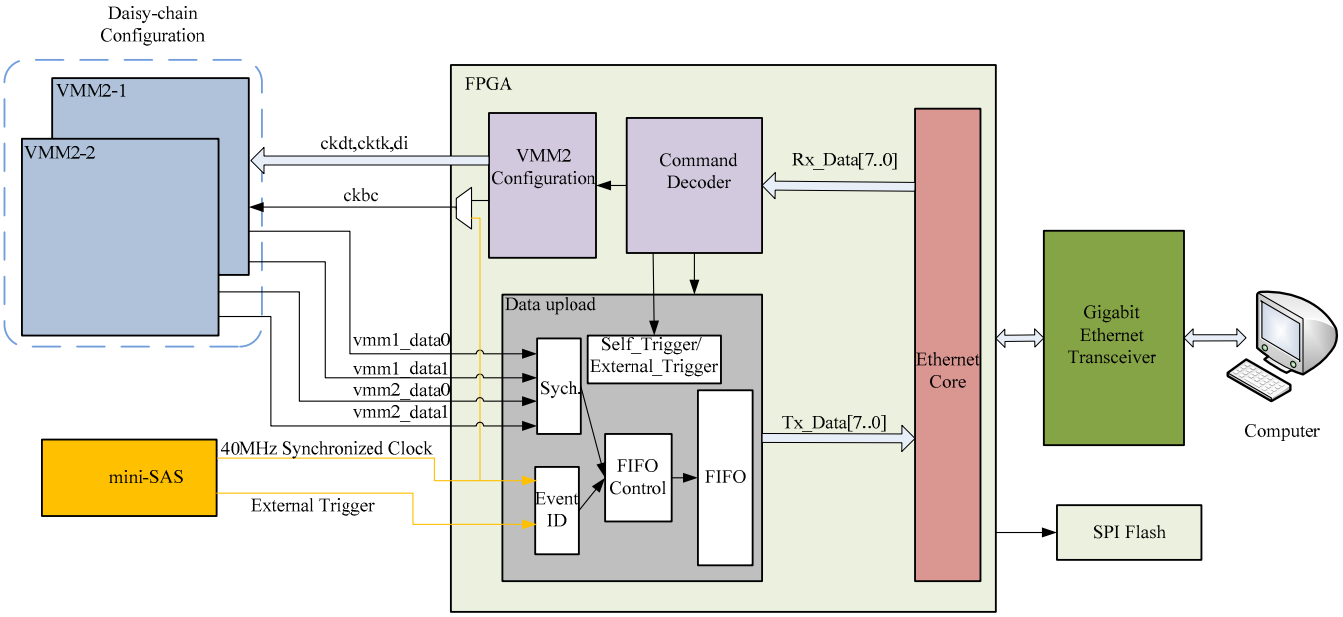

Fig. 1. Schematic block diagram of the DAQ prototype based on the Gigabit Ethernet interface.

C. *Data Format*

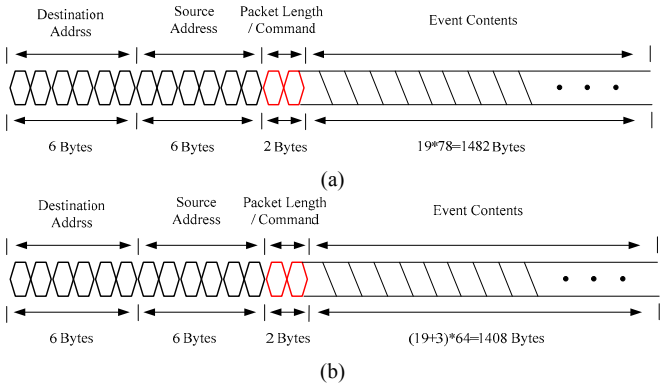

Fig. 2 The data format of an Ethernet packet without (a) and with (b) the external trigger.

The data format of an Ethernet packet is illustrated in Fig. 2. The data is transferred via an Ethernet interface. For a scenario without an external trigger shown in Fig. 2(a), each Ethernet packet has 78 events. Each event from VMM2 contains a total of 38 bits, shifted out in parallel to the *data0*, *data1* pin using 19 clock edges. The total number of an Ethernet packet are 1496 bytes, including a 6-bytes destination MAC address, a 6-bytes source MAC address, a 2-bytes user-defined token and 1482 bytes data from VMM2. For a case with an external trigger, however, an event Identification (ID) with 3 bytes is added after every event, which is generated via an internal counter driven by the external trigger signal. The total number of an Ethernet packet for this case are 1422 bytes, illustrated in Fig. 2(b). The 2-bytes token means a user-defined command when its value is higher than 1500. It also means an Ethernet packet length when lower than 1500.

III. Test Results

A. *Noise Test*

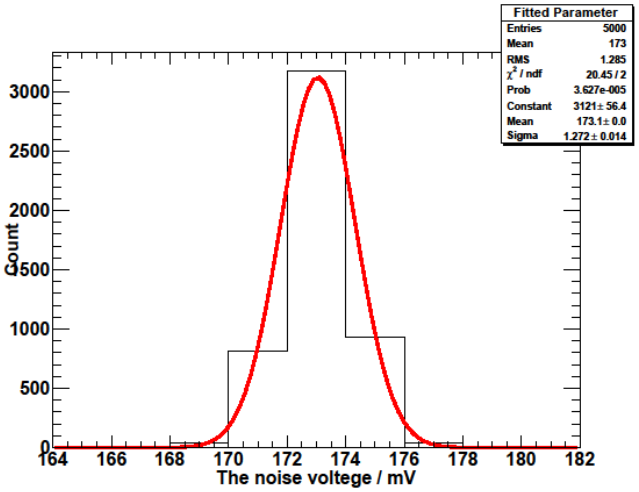

Fig. 3 The output noise of the DAQ prototype shielding the input charge signal.

The noise test is carried out after the VMM2 configuration. The signal from the monitor (MO) pin of the VMM2 is captured by a high-bandwidth Tektronix oscilloscope. Fig. 3 shows the output noise of the DAQ prototype. The noise voltage with a Gaussian distribution is plotted in a histogram. The root mean square (RMS) is less than 2 mV_{rms}. The noise is mainly contributed by the thermal noise of components, the 1/f noise which results from the parasitic capacitance in the PCB, and the high-frequency noise in digital components such as FPGA. The mean value is 173 mV, generated by a stable band-gap referenced baseline.

B. *VMM2 Linearity*

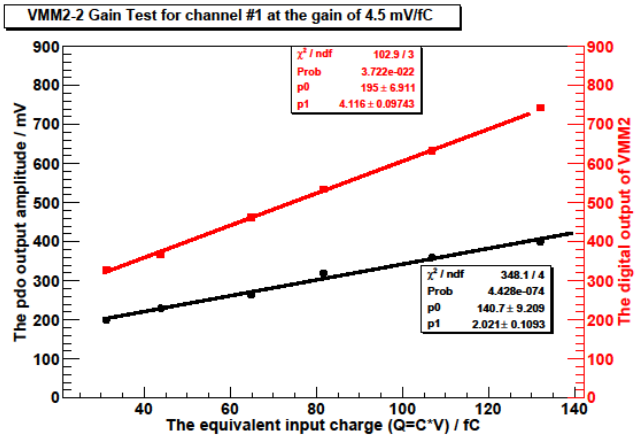

Fig. 4 The linearity test of a channel at the gain of 4.5 mV/fC.

The VMM2 chip consists of 64 front-end channels and digital processing circuit [5]. In our VMM2 configuration, the continuous mode is used. In the mode, the peak and the time detection convert the voltages into currents that are routed to the 10-bit ADC and 8-bit ADC respectively. The 10-bit ADC provides a high resolution A/D conversion for the peak value. The 8-bit ADC is applied to convert the peak timing, which is measured using a Time-Amplitude Conversion (TAC). The TAC stop signal occurs at the next clock period of a shared 12-bit Gray-code counter incremented using an external Bunch Clock (BC). Each channel is calibrated by a pulser and a 1.2 pF test capacitor. The pulser is adjustable with a global 10-bit DAC, triggered with an external test pulse clock. The digital value is sent to the VMM2 with the configuration bit sequence. Each channel has adjustable eight gains, offering higher analog dynamic ranges. For a given DAC value of the pulser and a given channel gain, we can obtain a histogram of the peak value. Stepping up the DAC value, a linearity test of the VMM2 channel is performed. The linearity test results are illustrated in Fig. 4. The Equivalent Input Charge (EIC) for the channel is described as Q=CV (1.2*AO). The slope of the fitted line means the actual channel gain we obtain, slightly less than the nominal value.

IV. Conclusion

In this paper, a DAQ prototype based on a Gigabit Ethernet interface has been built for the ATLAS small-strip Thin Gap Chamber (sTGC) Phase-I upgrade. The DAQ prototype consists of VMM2, FPGA and Gigabit Ethernet transceiver. The VMM2 performance is discussed in detail. In the early upgrade, the DAQ prototype will be used for the sTGC performance test.

References

[1] ATLAS Collaboration, The ATLAS Experiment at the CERN Large Hadron Collider, JINST **3** S0800S (2008).

[2] ATLAS Collaboration, New Small Wheel Techincal Design Report, No. CERNLHCC-2013-006 or ATLAS-TDR-020, 1995.

[3] S. Majewski, et al., A Thin multiwire chamber operating in the high multiplication mode, Nucl. Instr. Meth. A **217**, 265 (1983).

[4] G. De Geronimo et al., VMM1-An ASIC for micropattern detectors, IEEE Trans. Nucl. Sc., **60**, 2314 (2012).

[5] https://twiki.cern.ch/twiki/pub/Atlas/NSWelectronics/VMM2_datasheet_v15.pdf