New updates on the ATLAS ROD board implementation for Pixel Layer 1 and Layer 2

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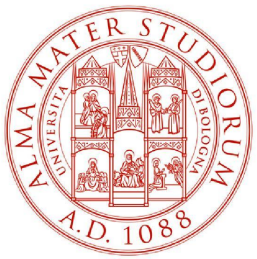
June 9, 2016



About this Poster

The poster main intent is to present:

- the **Read-Out Driver** (ROD) Board developed for the **ATLAS** experiment at **CERN**;
- the **ATLAS Pixel Detector** Read-Out Chain;
- the **technological challenges** which brought to the design of the **Read-Out Driver** (ROD) Board;
- **motivation** for the upgrade of the Read-Out system;
- **status** and results of the new **ROD**.

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Introduction and motivations

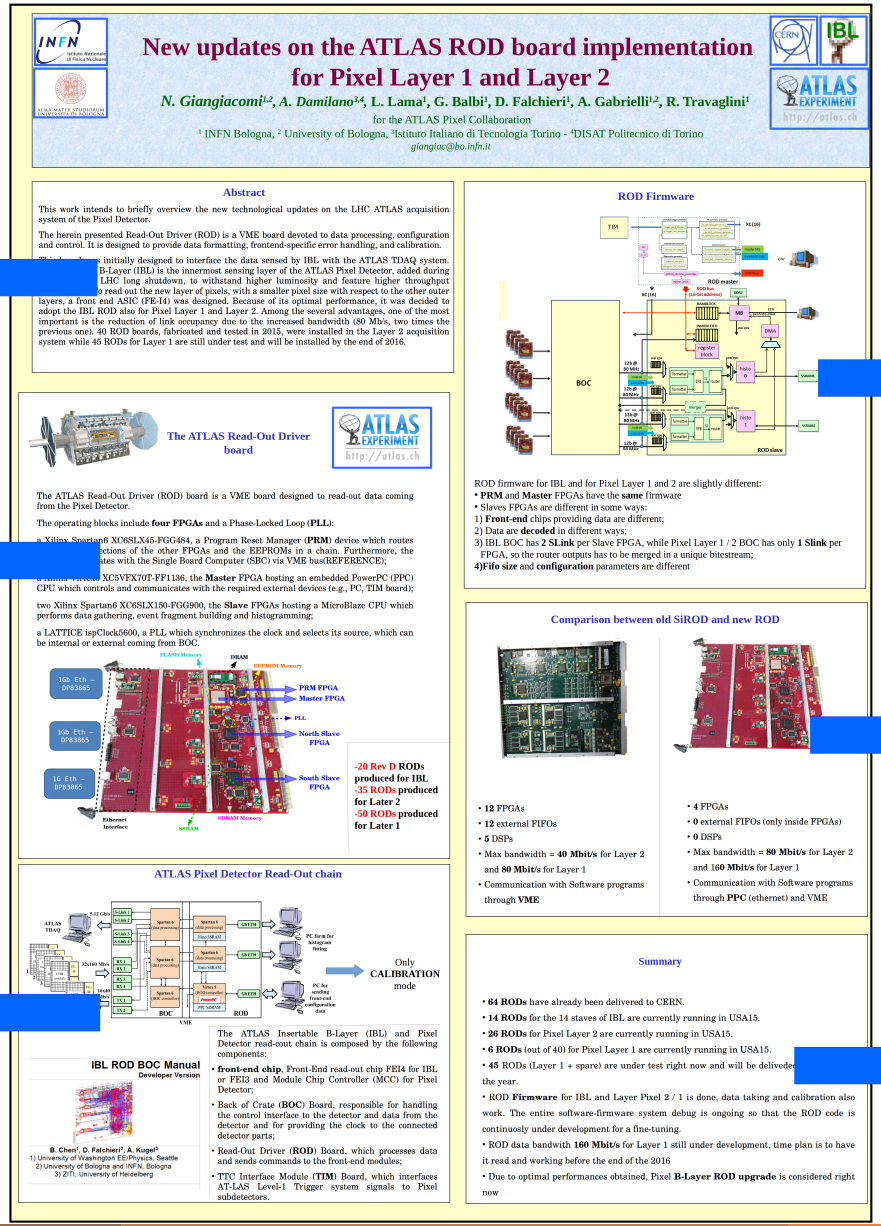
ROD components description

Read-Out chain overview

ROD Firmware overview

Comparison between old and new ROD

Conclusions and results



New updates on the ATLAS ROD board implementation for Pixel Layer 1 and Layer 2

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for the ATLAS Pixel Collaboration

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Abstract

This work intends to briefly overview the new technological updates on the LHC ATLAS acquisition system of the Pixel Detector.

The herein presented Read-Out Driver (ROD) is a VME board devoted to data processing, configuration and control. It is designed to provide data formatting, frontend-specific error handling, and calibration.

initially designed to interface the data sensed by IBL with the ATLAS TDAQ system. B-Layer (IBL) is the innermost sensing layer of the ATLAS Pixel Detector, added during LHC long shutdown, to withstand higher luminosity and feature higher throughput read out the new layer of pixels, with a smaller pixel size with respect to the other outer layers, a front end ASIC (FE-I4) was designed. Because of its optimal performance, it was decided to adopt the IBL ROD also for Pixel Layer 1 and Layer 2. Among the several advantages, one of the most important is the reduction of link occupancy due to the increased bandwidth (80 Mb/s, two times the previous one). 40 ROD boards, fabricated and tested in 2015, were installed in the Layer 2 acquisition system while 45 RODs for Layer 1 are still under test and will be installed by the end of 2016.

The ATLAS Read-Out Driver board

The ATLAS Read-Out Driver (ROD) board is a VME board designed to read-out data coming from the Pixel Detector.

The operating blocks include **four FPGAs** and a Phase-Locked Loop (**PLL**):

a Xilinx Spartan6 XC6SLX45-FGG484, a Program Reset Manager (**PRM**) device which routes ections of the other FPGAs and the EEPROMs in a chain. Furthermore, the ates with the Single Board Computer (SBC) via VME bus(REFERENCE);

XC5VFX70T-FF1136, the **Master** FPGA hosting an embedded PowerPC (PPC) CPU which controls and communicates with the required external devices (e.g., PC, TIM board);

two Xilinx Spartan6 XC6SLX150-FGG900, the **Slave** FPGAs hosting a MicroBlaze CPU which performs data gathering, event fragment building and histogramming;

a LATTICE ispClock5600, a PLL which synchronizes the clock and selects its source, which can be internal or external coming from BOC.

-20 Rev D **RODs produced for IBL**
-35 **RODs produced for Later 2**
-50 **RODs produced for Later 1**

ATLAS Pixel Detector Read-Out chain

Only **CALIBRATION** mode

IBL ROD BOC Manual
Developer Version

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1) University of Washington EE/Physics, Seattle
2) University of Bologna and INFN, Bologna
3) ZITI, University of Heidelberg

The ATLAS Insertable B-Layer (IBL) and Pixel Detector read-out chain is composed by the following components:

- **front-end chip**, Front-End read-out chip FEI4 for IBL or FEI3 and Module Chip Controller (MCC) for Pixel Detector;
- Back of Crate (**BOC**) Board, responsible for handling the control interface to the detector and data from the detector and for providing the clock to the connected detector parts;
- Read-Out Driver (**ROD**) Board, which processes data and sends commands to the front-end modules;
- TTC Interface Module (**TIM**) Board, which interfaces AT-LAS Level-1 Trigger system signals to Pixel subdetectors.

ROD Firmware

ROD firmware for IBL and for Pixel Layer 1 and 2 are slightly different:
- **PRM** and **Master** FPGAs have the **same** firmware
- Slaves FPGAs are different in some ways:

1) **Front-end** chips providing data are different;
2) Data are **decoded** in different ways;
3) IBL BOC has **2 SLink** per Slave FPGA, while Pixel Layer 1 / 2 BOC has only **1 Slink** per FPGA, so the router outputs has to be merged in a unique bitestream;
4)Fifo size and **configuration** parameters are different

Comparison between old SiROD and new ROD

- **12** FPGAs
- **12** external FIFOs
- **5** DSPs
- Max bandwidth = **40 Mbit/s** for Layer 2 and **80 Mbit/s** for Layer 1
- Communication with Software programs through **VME**

- **4** FPGAs
- **0** external FIFOs (only inside FPGAs)
- **0** DSPs
- Max bandwidth = **80 Mbit/s** for Layer 2 and 160 **Mbit/s** for Layer 1
- Communication with Software programs through **PPC** (ethernet) and VME

Summary

- **64 RODs** have already been delivered to CERN.
- **14 RODs** for the 14 staves of IBL are currently running in USA15.
- **26 RODs** for Pixel Layer 2 are currently running in USA15.
- **6 RODs** (out of 40) for Pixel Layer 1 are currently running in USA15.
- **45** RODs (Layer 1 + spare) are under test right now and will be delivede the year.
- ROD **Firmware** for IBL and Layer Pixel 2 / 1 is done, data taking and calibration also work. The entire software-firmware system debug is ongoing so that the ROD code is continuosly under development for a fine-tuning.
- ROD data bandwith **160 Mbit/s** for Layer 1 still under development, time plan is to have it read and working before the end of the 2016
- Due to optimal performances obtained, Pixel **B-Layer ROD upgrade** is considered right now

The End