A Hybrid Analog-digital Integrator for EAST Device

Y. Wang, Z.S. Ji, Z.C. Zhang, S. Li, F. Wang, X.Y. Sun

***Abstract*–A hybrid analog-digital integrator has been developed to be compatible with the long pulse plasma discharges on Experimental Advanced Superconductor Tokamak (EAST), in which a pair of analog integrators are used to integrate the input signal by turns to reduce the error caused by the leakage of integration capacitors, and the outputs of two integrators can be combined to construct a continuous integration signal by a Field Programmable Gate Array (FPGA) built in the digitizer. The integration drift is almost linear and stable in controlled temperature, so a period of typically 50 s is used to determine the effective drift slope, which is used to rectify the integration signal in real time. The data integrated in the internal FPGA can be directly transferred into the reflective memory installed in the same PCI eXtensions for Instrumentation (PXI) chassis. The test results show that the processed integration drift is less than 200 uVs during 1000 s integration, which will meet the accuracy of magnetic diagnostics in EAST experimental campaigns.**

I. Introduction

Magnetic diagnostics (MDs) [1] provides one of the most important diagnostics to the operation and plasma control in tokamaks. MDs are normally composed of a series of different kinds of inductive sensors, from which integrators are used to convert acquired voltages to field strength.

EAST is aimed at high performance plasma for long pulse up to 1000 s or longer [2, 3]. The development of the integrators with very low drift for MDs is quite important. However, the integrators drift will be accumulated during integration. The traditional analog integrator circuit is not suitable for the long pulse device. One of the main difficulties of analog integrators is how to reduce the integration drift [4, 5], which is caused by the offset and temperature drift of the circuit components, leakage of the integration capacitor and noise, etc. On EAST device, in order to minimize the drifts, some methods have already been used on analog integrators to deal with the linear drift caused by the amplifier offset and temperature [4], which work well on time scale in hundreds of seconds, but the leakage of the feedback capacitor and possible saturation of the single integrator should be taken into account for the very long time operation.

Therefore, it appears that the requirements for the signal integration towards the long pulse discharges cannot satisfy with purely analog integrators, other methods must be taken into account, such as digital integrators [6-11]. A digital chopper integrator has been developed for Wendelstein 7-X, which achieves very low drift rate of less than 0.1 uVs/s [8], but requires about 100 ms for data processing [9]. In order to reduce the latency to 100 us, real time progress on FPGA have been tested and satisfy this requirement [10, 11], but the 16-bit ADC is not good enough to control the drift. So the requirement of the digital integrator is high speed 24-bit ADC sampling with FPGA real time process [11], which is a big challenge and not easy to realize.

A kind of hybrid integrators [12] has been developed on Joint European Torus (JET), in which two integrators are used to work by turns, and the outputs of the two integrators can be digitized by ADC and can be combined to construct a continuous real-time integral of the source signal by digital processor, so that the leakage and saturation can be avoided.

In this article, we aim to realize this kind of hybrid integrator of real time integration on PXI platform for its numerous kinds of digitizer and FPGA modules and easy implementation with LabVIEW. A multifunction module integrated with ADC and FPGA was used to realize the hybrid analog-digital integrator and the performance test and analysis has been demonstrated.

II. Design

A. Architecture

The architecture diagram of hybrid analog-digital integrator is shown in Fig. 1. The induced signal is chopped and integrated by the integrator chopper firstly, and then the chopped signal is sampled into digital processor by analog to digital converter (ADC), in which efficient algorithms can be used to realize the integration and reduce the integration drift. As we focused on real time processing, the integration is done in FPGA and integration data is transferred to Plasma Control System (PCS) for real time control through RFM network.

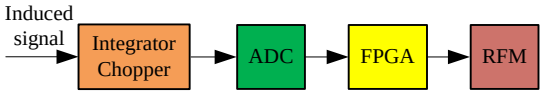

Fig. 1. Architecture of the hybrid integrator.

For ADC and FPGA processing, we selected the NI PXI-7854R [13] multifunction reconfigurable input/output (RIO) module, which features a user-programmable Virtex-5 LX110 FPGA chip for onboard processing, 8 analog inputs of independent sampling rates up to 750 kHz, 16-bit resolution and ±10 V input range and 96 digital lines configurable as inputs, outputs, counters, or custom logic at rates up to 40

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MHz, so this module is quite suitable to realize hybrid integration. GE cPCI-5565 [14] Reflective Memory PXI module provides an optical ring-based, ultra high-speed shared memory network solution. It allows a distributed network to share real-time data at a deterministic rate, regardless of bus structures and operating systems. The NI PXI-8133 [15] is a high-performance 1.73 GHz quad-core embedded controller for use in PXI systems and installed LabVIEW RT operation system, it is ideal for the hybrid integrator to process and write data to RFM card. All the modules above can be installed in one 8-slot 3U NI PXI-1082 chassis [16].

B. *Integrator Chopper*

The chopper consists of the matched resistor Rs, the analog switches and the integrator cells, which is shown in Fig. 2.

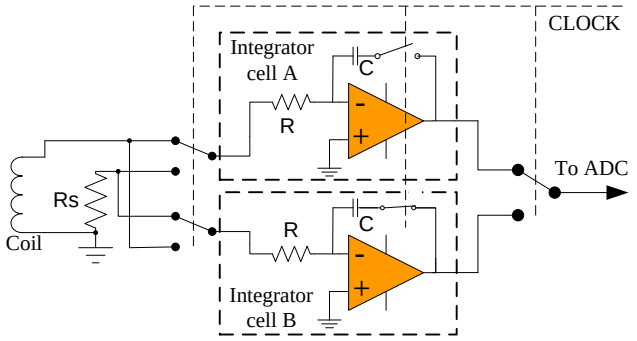

Fig. 2. Schematic of the integrator chopper.

Two analog integrators was used, integrator cell A, connected to the coil and the other, integrator cell B, to a resistor Rs via a set of analog switches. After a certain period of time, which is called chopping time τ, integrator cell B is switched to the coil, and integrator cell A is switched to the resistor and reset. When the next τ comes, the resetting and switching process is repeated.

The resistor Rs is used to match the dc resistance of the coil and wires, its value is about 20 Ω.

The switches are very important for the integrator chopper, and basically four criteria are of importance for the switch selection: dual supply operation, low switch time, low on resistance and low charge injection into the signal path. Relays are not suitable for this chopper due to their long switching time. For the actually chosen MAX314 [17] the switch dual supply operation is from ±4.5 V to ±20 V, typically switch time is 70 ns, on resistance is 6.5 Ω and the charge injection per switching process is 20 pC.

The integrator cells are the key issues of the integrator chopper. The integrator drift should be small and stable, so that it can be easy to process in the FPGA. The integrator cell is composed of an operational amplifier, an input resistor R and a capacitor C. In order to minimize the drifts, the 1‰ high precision resistors and polypropylene capacitors of low leakage current and dual zero drift operational amplifiers LTC1151 [18] are chosen. LTC1151 has a typical offset voltage of 0.5 uV, an input offset current of 20 pA, and an average input offset drift of 0.01 uV/ °C. These characteristics are ideal to realize a low drift integrator.

The integrator chopper board was developed in-house, which has 8 analog inputs and compatible SCSI-68 interface with PXI-7854R for easy connection.

C. *Algorithm of Integrator Chopper*

The principle of the hybrid integrator is shown in Fig. 3. V_i is the raw signal, so the result of integration $V_s = \int V_i dt$. CLK is chopping clock signal to control the chopper frequency. After being chopped by the switches and integrated by integrator cells, the integration result of each chopping time becomes

$$V_s(\tau) = \frac{1}{RC}\int_0^{\tau} V_i dt \qquad (1)$$

By integration on FPGA the outputs of the two integrators can be combined to construct a continuous real-time integral of the source signal.

$$V_s = \frac{1}{RC}\int_0^{\tau} V_i dt + \frac{1}{RC}\int_{\tau}^{2\tau} V_i dt + \frac{1}{RC}\int_{2\tau}^{3\tau} V_i dt + \ldots \qquad (2)$$

The clock signal delivered by the PXI-7854R FPGA module is at the cycle of 50 s, so the chopping time τ is 25 s. The sampling rate is 500 kHz and every 50 samples are used to get a mean value to reduce noise, so the transmission rate is 10 kHz.

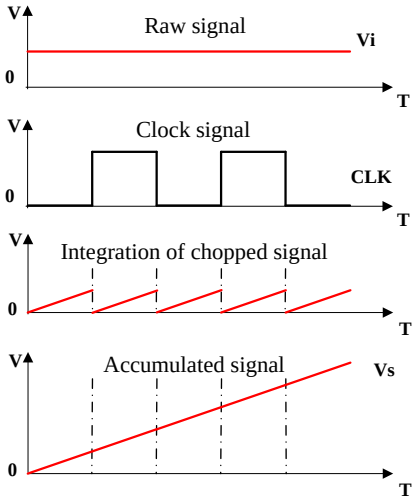

Fig. 3. Principle of the chopper.

D. *Linear Drift Compensation*

The chopping method of using two integrators to work by turns is a good way to avoid leakage and saturation. While there is still some drift caused by amplifier offset and noise, but it changes slowly in a certain time when the environment is stable, which means that the drift is almost linear, so the previous drift rate can be used to deduct the linear drift in next period, then the integration drift can be reduced greatly.

Considering the countdown of each EAST experiment shot is 60 s, a period of 50 s (a chopping clock cycle) is used to determine the effective linear drift rate, there should be no induced signal during that interval as otherwise the calculated rate is not the true integrator drift rate.

The drift is measured by just taking two measurements at a certain period of time apart. This algorithm is shown in Fig. 4, which has three steps.

1. After receiving a trigger signal (at time -60 s), a certain period (typically 1 s) sample result of the integrator output is acquired, and the mean value V_1 can be calculated, then after a period time T_0 (typically 50 s), another certain period sample result is acquired, and the mean value V_2 can be calculated, so the drift rate $k = (V_2 - V_1)/T_0$, as shown in Fig. 4(a).
2. The drift rate k is used to calculate the drift V_d of each process interval, as shown in Fig. 4(b). $V_d[i] = k \times i \times \Delta t$, where Δt is the time of process interval. If the process rate is 10 kHz, Δt is 100 us.
3. The processed result is

$$V_o[i] = V_s[i] - V_d[i] \qquad (3)$$

By linear compensation, the affect of linear drift is almost eliminated, as showed in Fig. 4(c).

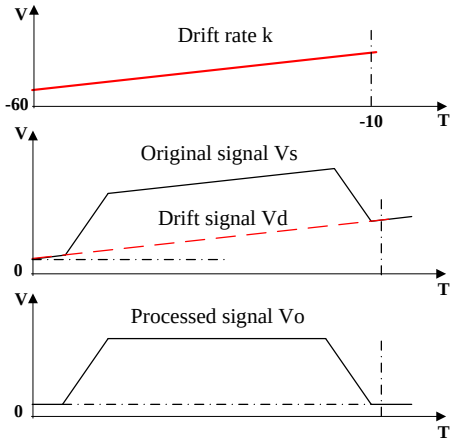

Fig. 4. Algorithm of linear drift compensation.

E. Software Structure

The software structure of hybrid integrator includes three parts:

Program on host provides the user interface, which includes display and parameters setting, such as sampling rate, chopping clock cycle and acquisition time.

Program on LabVIEW FPGA includes sampling and accumulating the chopped integration signal, which is shown in Fig. 5(a). The chopper clock signal is also generated by FPGA.

Program on LabVIEW RT includes receiving parameters from program on PC, correcting drift, and transferring the integration data to RFM, as shown in Fig. 5(b).

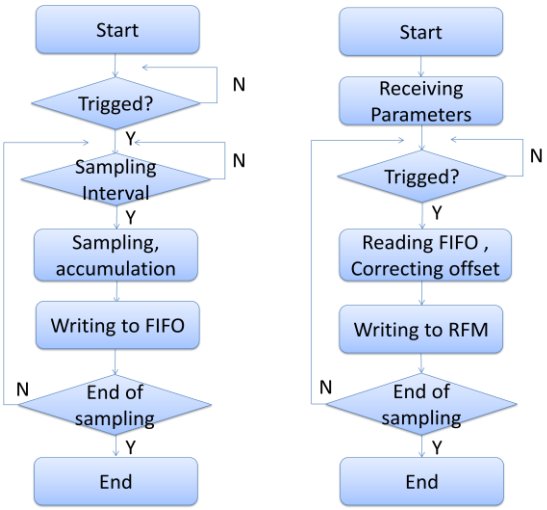

Fig. 5. Program flow chart of the hybrid integrator.
(a) Program on FPGA, (b) Program on LabVIEW RT.

III. Performance

A hybrid analog-digital integrator of 20 ms integration time constant was tested. R = 20 kΩ, C = 1 uF and the chopping time τ = 25 s.

A. RFM Test

The format of data on RFM is just a memory location containing the last integration value. The way to exchange data between hosts in the same RFM network is direct memory access (DMA). We verified that the LabVIEW FPGA and RT can manipulate the above process at the rate of 10 kHz, and we also checked that an RFM receiver can receive all 10k samples without getting lost.

B. Function Test

.A 2 mV power source was applied to the integrator input, and the integration result is about 200 uVs after 100 s integration, which shows that the integration function is right, as shown in Fig. 6.

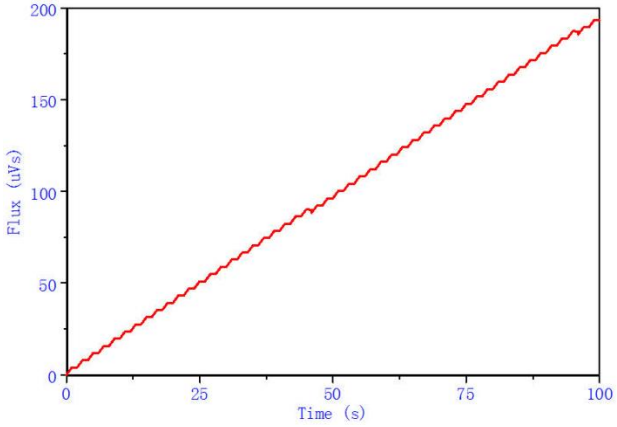

Fig. 6. 100 s integration when the input is connected to a 2 mV source.

C. *Drift Test*

When the input is shorted, 5 shots of 1000 s integration drifts of the digital integrator are less than 150 uVs, which shows good performance, as shown in Fig. 7.

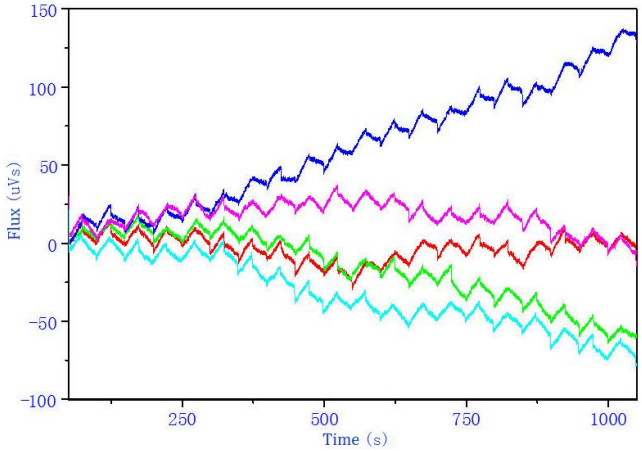

Fig. 7. Integration drifts of 1000 s when the input is shorted.

IV. Conclusion and Future Work

This work clearly demonstrates that a kind of hybrid analog-digital integrator based on PXI platform has been developed, which uses two analog integrator cells to work by turns to avoid leakage of capacitors, and has 10 kHz real time data transmission by RFM and low drift of typically 0.15 uVs/s.

Future work requires more effort on noise control and improvement of the integration and stability of the integrator chopper board and more test on EAST device.

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