Real Time controller for R&D on ITER Ion Cyclotron Heating & Current Drive Source

Sriprakash Verma, Kumar Rajnish, Dipal Soni, Hriday Patel, Aparajita Mukherjee, Rajesh Trivedi, Raghuraj Singh

***Abstract*–INDA is responsible for development & delivery of total 9 no. of RF sources for ITER Ion cyclotron Heating & Current Drive (ICH & CD) system [1]. To validate the design an R&D program has been initiated. Each ICH & CD source consist of two chains of amplifier and each chain composed of low power RF section, one medium power solid state amplifier followed by two tuned high power tube (tetrode/diacrode) based amplifiers, high voltage/high current power supplies and control system. A dedicated data acquisition and control system has been developed based on Real Time (RT) PXI controller. To achieve the performance of RF source as required by ITER, anode voltage and voltage standing wave ratio (VSWR) control loops are implemented on Field Programmable Gate Array (FPGA) module. Interlock logic is running on FPGA to protect high power RF tubes and different subsystems. Two mode of data acquisition function is implemented on NI PXI-8108 RT controller (Embedded RTOS Controller). For logging different signals and status of subsystems, normal acquisition at 1ms sampling rate is implemented. For acquiring different events before fault/RF shutdown, trigger based fast data acquisition at 1µs sampling rate is implemented.**

I. Introduction

THE Ion Cyclotron Heating and Current Drive system is one of the most important auxiliary heating and current drive systems for ITER Experiment. ITER requirement is to have 8 independent RF sources in the range of 35-65MHz, having 2.5 MW power output at VSWR of 2.0 and Bandwidth of +/- 1MHz. Each RF Source should be operated independently as well as it should be synchronized with ITER central control system. Fig. 1 shows the overall block diagram of ICH & CD Source. ICH&CD source will be consists of two independent chain of amplifiers and one combiner at the output. Each chain is composed of voltage variable attenuator, voltage variable phase shifter, Sold State Power Amplifier (SSPA), driver amplifier (HPA2), final stage amplifier (HPA3), different auxiliary power supplies and Local Control Unit (LCU). For R&D purpose single chain of amplifiers having capability of 1.5 MW at VSWR 2:1 in the frequency range 35 – 65 MHz is considered.

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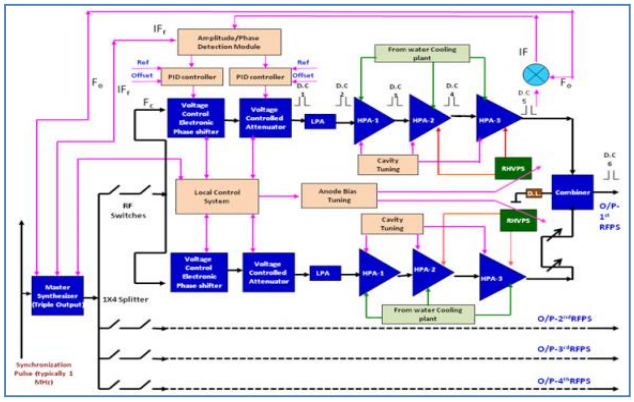

Fig. 1. Block Diagram of ICH&CD Source

A. Local Control Unit

Local Control Unit is designed and developed for demonstration of performance of the RF sources. To ensure reliable and safe operation of the entire system, PLC/PXI based architecture is used. For development of application program, LabVIEW software tool is used. NI PXI-8108 [3] RT controller is used for real time control purpose; whereas PXI-6255 [4] I/O board is used for data acquisition at 1ms sampling frequency and PXI-6133[5] I/O board is used for event based data acquisition at 1µs sampling frequency. Sequential control system is designed and developed using Schneider PLC hardware for biasing of electrodes of high power vacuum tubes (Tetrode/Diacrode). Unity pro software tool is used for coding of PLC. PXI-7841R [2] FPGA board is used to implement the internal protection function for the system against critical fault of RF and power supplies, whose response time is less than 10 µs. Real time control loops are developed for stable and constant power complying with ITER requirement. For fault/offline analysis, event based acquisition and logging functionality is provided that acquires and logs data at 1µs sampling rate for 100ms pre and post time. During the RF Shot, normal acquisition and logging for all channels are provided with 1ms sampling rate. Further, online display for user selectable 8 channels is provided on main screen tab of the application program. All the operational and monitoring parameters are continuously updated on main screen to give the real time status of the system. Fig. 2 shows the LCU architecture.

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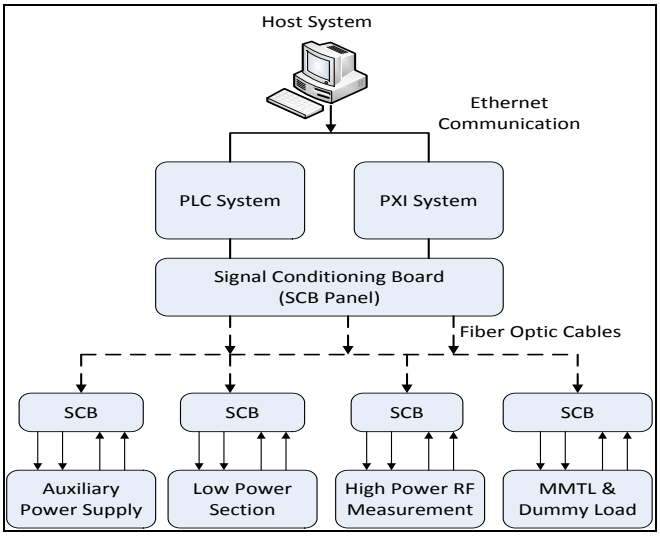

Fig. 2 . Local Control Unit Architecture

II. REAL TIME CONTROL LOOP

To demonstrate the ITER requirement, constant and stable 1.5 MW output from a single chain of amplifiers, even with variable load condition (up to VSWR 2) is required which is one of critical requirements for ITER RF Source. To comply with such operation, two real time feedback control loops are employed – (1) Anode voltage regulation loop for optimizing anode & screen grid dissipation and (2) VSWR loop for making constant output power. NI-7841R FPGA board is used as hardware for the implementation of the real time control loop in Local Control Unit.

A. Anode voltage (V_A) regulation loop

Generally plasma load is dynamic in nature and affect the performance of RF source by creating VSWR situation. To limit dissipation in the high power vacuum tubes and achieving maximum efficiency of the entire system, the anode voltage is regulated over a wide range of load changes. At the same time this loop protects the tube by reducing the RF power instead of switching it off. Anode power dissipation (APD) and Screen grid current (I_{g2}) are directly coupled to the anode voltage and RF power. Normally I_{g2} increases during VSWR condition, which can be controlled by increasing Anode Voltage (V_A). This regulation system is tuned to keep I_{g2} constant at its optimum value by adjusting the anode voltage to its limiting value. In this way the efficiency of the system can also be optimized.

If for any reason V_A cannot be increased further and I_{g2} reaches a second limit (I_{g2lim}), the RF drive power is decreased keeping I_{g2} constant at upper level. This I_{g2} regulation works as long as dissipated power APD remains under limit. As it crosses the limiting value, anode voltage will be reduced immediately. Fig. 3 shows the characteristics of anode voltage regulation loop.

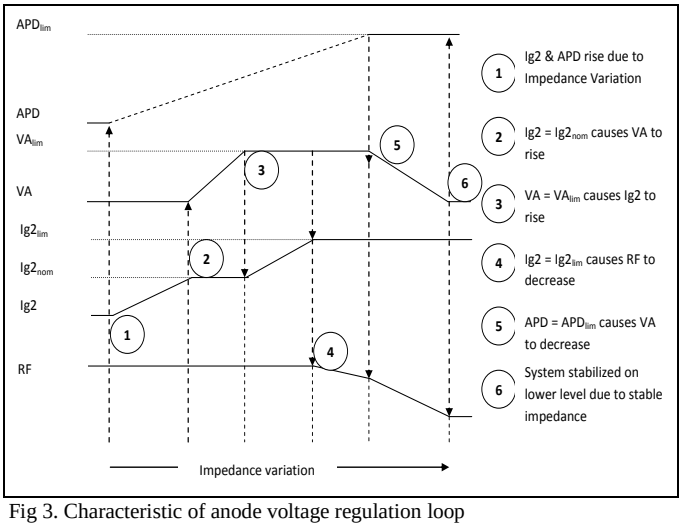

Fig 3. Characteristic of anode voltage regulation loop

There are some constant parameters used in anode voltage and RF regulation loop. These parameters are anode power dissipation limit (APD limit), ramp rate for anode voltage, operating anode voltage, ramp rate for RF drive, Minimum RF drive, first limit of screen grid current (I_{g2nom}), RF maximum drive, second limit of screen grid current (I_{g2lim}), maximum value of operating anode voltage. During initialization of V_a loop, calculated APD is compared with limiting value of APD. If calculated APD > APD limit, then anode voltage and RF drive power both will be decreased as per their ramp rate up to the operating anode voltage and minimum RF reference power respectively. If calculated APD < APD limit then screen grid current (I_{g2}) parameter is checked for further action.

If $I_{g2} < I_{g2nom}$ then RF drive power is increased and if $I_{g2} > I_{g2nom}$ then I_{g2} is compared with I_{g2lim} for further action. Now if $I_{g2nom} < I_{g2} < I_{g2lim}$ then anode voltage should be increased up to the limiting anode voltage. Code is continuously checking the changes in screen grid current, if it is greater than certain predefined level then only anode voltage change is applicable. If $I_{g2} > I_{g2lim}$ then RF drive should be decreased up to minimum RF level. One analog output signal is generated as a new reference set point for anode voltage.

B. VSWR Loop

VSWR is voltage standing wave ratio and derived from forward power (FP) and reflected power (RP).

$$VSWR = (\sqrt{FP}+\sqrt{RP})/(\sqrt{FP}-\sqrt{RP}) \qquad (1)$$

The output power is regulated for the requested power level by comparing the measured feedback signal with the reference level from Graphical User Interface (GUI) taking VSWR into account. Fig. 4 shows the flow chart of VSWR regulation loop. The output power (Pload) is influenced by VSWR and to make the constant output power, input drive power should be adjusted. Nominal power P_{nom} is the adjusted output power for VSWR greater than 1 & less than 2. At 2<VSWR<3, the reflected power is kept constant at 165KW.

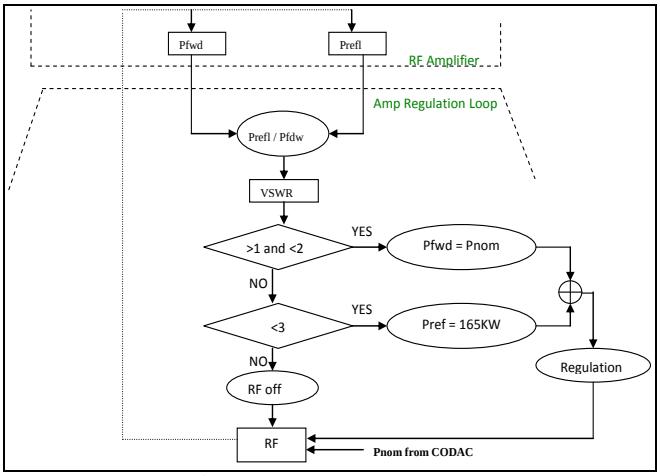

Fig. 4. Flow chart of VSWR regulation loop

At VSWR = 3 or more, RF power is blocked to avoid more reflection to the system.

III. INTERLOCK LOOP

Interlock loop is required for fast protection of RF source system. Interlocks are hard wired system and acts within 10µs. All the digital inputs are continuously monitored and if found healthy then RF pulse will be generated according to predefined RF shot parameters. If the operating parameter crosses the maximum level specified by system designer, RF and associated power supply will be withdrawn.

IV. DATA ACQUISITION AND MONITORING

There are two types of data acquisition has been incorporated in Local control unit. First is 40 channel continuous data acquisition at 1ms sampling frequency using PXI-6255 I/O board and second is event based data acquisition with 100 ms pre-post data at 1µs sampling frequency using PXI-6133 I/O board. The acquired data is stored on RT controller hard drive and then transferred to HOST system. Voltage & current of different power supplies, forward power, reflected power and status of different digital signals are continuously monitored on Graphical User Interface. User can select any 8 channels to see online graph of 100 sec data at 1ms sapling frequency.

V. OTHER FEATURES OF LCU

- Configuration module has been developed for calibration of different voltage & current monitoring signals, forward power & reflected power, setting of low power section variables like coarse frequency, fine frequency, coarse power etc. and threshold setting of different power supplies.
- User administrator module has been developed for defining the login rights. User can login either as an administrator or as an operator.
- Interlock detection and latching function in sequence of occurrence of faults.

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