The ALICE C-RORC GBT card, a prototype readout solution for the ALICE upgrade.

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***Abstract*–ALICE (A Large Ion Collider Experiment) is the detector system at the LHC (Large Hadron Collider) optimized for the study of heavy-ion collisions at interaction rates up to 50 kHz and data rates beyond 1 TB/s. Its main aim is to study the behavior of strongly interacting matter and the quark gluon plasma. ALICE is preparing a major upgrade and starting from 2021, it will collect data with several upgraded sub-detectors (TPC, ITS, Muon Tracker and Chamber, TRD and TOF). The ALICE DAQ read-out system will be upgraded as well, with a new read-out link called GBT (GigaBit Transceiver) with a max. speed of 4.48 Gb/s and a new PCIe gen.3 x16, interface card called CRU (Common Read-out Unit). Several test beams have been scheduled for the test and characterization of the prototypes or parts of new detectors. The test beams usually last for a short period of one or two weeks and it is therefore very important to use a stable read-out system to optimize the data taking period and be able to collect as much statistics as possible. The ALICE DAQ and CRU teams proposed a data acquisition chain based on the current ALICE DAQ framework in order to provide a reliable read-out system. The new GBT link, transferring data from the front-end electronics, will be directly connected to the C-RORC, the current read-out PCIe card used in the ALICE experiment. The ALICE DATE software is a stable solution in production since more than 10 years. Moreover, most of the ALICE detector developers are already familiar with the software and its different analysis tools. This setup will allow the detector team to focus on the test of their detectors and electronics, without worrying about the stability of the data acquisition system. An additional development has been carried on with a C-RORC-based Detector Data Generator (DDG). The DDG has been designed to be a realistic data source for the GBT. It generates simulated events in a continuous mode and sends them to the DAQ system through the optical fibers, at a maximum of 4.48 Gb/s per GBT link. This hardware tool will be used to test and verify the correct behavior of the new DAQ read-out card, CRU, once it will become available to the developers. Indeed the CRU team will not have a real detector electronics to perform communication and performance tests, so it is vital during the test and commissioning phase to have a data generator able to simulate the FEE behavior. This contribution will describe the firmware and software features of the proposed read-out system and it will explain how the read-out chain will be used in the future tests and how it can help the development of the new ALICE DAQ software.**

I. Introduction

ALICE [1] (A Large Ion Collider Experiment) is preparing a major upgrade and for the RUN3 in 2021 it will collect data with several upgraded detectors: TPC (Time Projection Chamber), ITS (Inner Tracking System), Muon Tracker and Chamber, TRD (Transition Radiation Detector) and TOF (Time Of Flight). The terms LS1, LS2 and LS3 refer to the LHC Long Shutdowns in 2013-14 and anticipated in 2019-20 and 2024-26, during which the detector upgrades occur. Run 1, Run 2, Run 3 and Run 4 refer to the periods of data taking operation of ALICE in between these shutdowns.

The ALICE DAQ readout system will be upgraded as well to cope with the higher data throughput and will be part of a new computing system called O2 [2], combining the functionalities of the present DAQ, HLT and Offline systems. A new PCIe card called CRU [3] (Common Readout Unit) and a new readout link called GBT [4] (GigaBit Transceiver) will be used to collect data from the front-end electronics of several detectors.

TABLE I. OVERVIEW OF THE ALICE DETECTORS AND THEIR READOUT LINKS

Detector Code	Link type	Number of links	Read-out board
ACO	DDL1	1	C-RORC
CPV	DDL1	6	C-RORC
CTP	GBT	14	CRU
EMC	DDL2	20	C-RORC
FIT	DDL2	2	C-RORC
HMP	DDL1	14	C-RORC
ITS	GBT	495	CRU
MCH	GBT	550	CRU
MFT	GBT	304	CRU
MID	GBT	32	CRU
PHS	DDL2	16	C-RORC
TOF	GBT	72	CRU
TPC	GBT	5832	CRU
TRD	Custom	1044	CRU
ZDC	GBT	1	CRU

II. The motivation

In 2016 several test-beams have been scheduled to characterize prototypes or parts of new detectors and their new FEE (Front End Electronics). A test-beam session could last a couple of weeks maximum, so it is important to have a stable readout system, to collect as much statistics as possible.

The new readout card, CRU, won't be available in time for these detector tests, and the new readout software and firmware are still under development. For these reasons the ALICE DAQ and CRU groups proposed a prototype readout system based on ALICE DATE [5] (Data Acquisition and Test

Environment) and the C-RORC [6] (Common Readout Receiver Card, the read-out card currently used in ALICE) to collect data during the tests. DATE is a stable solution, in production since more than 15 years. Detector teams can rely on its performance and stability, focusing on their test of the detector hardware.

III. The C-RORC Hardware

The prototype readout system is based on the C-RORC (figure 1).

The C-RORC is a PCIe card equipped with:

- 12 optical links.
- 1 PCIe gen.2 x 8.
- 1 XILINX VIRTEX6 FPGA.
- Some general purpose I/O.

The card is very stable and it is in production for data taking since 2014.

Fig. 1. C-RORC hardware: on the left the optical transceivers, in the center the FPGA, under the fan, and the PCIe interface.

IV. The GBT Protocol

The GBT protocol (figure 2) encapsulates in one bi-directional optical fiber, 3 different streams:

- Data.
- Trigger.
- Slow Control.

The main components are:

- the GBTx chip, or GBT-FPGA,
- the versatile link.

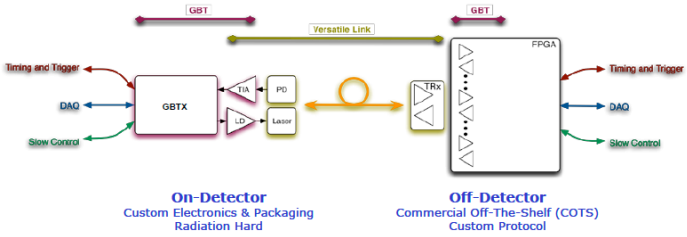

Fig. 2. Main component of the GBT: GBT-x chip, versatile link and the GBT-FPGA. On the left and right side the 3 different streams (Trigger, DAQ and Slow Control) that the GBT encapsulates in a single link.

This link establishes a point-to-point connection that can work in the harsh radiation environment of high-energy physics experiments at LHC.

V. The C-RORC and the GBT

In RUN3 the experiment will support mainly 2 different readout protocols to collect data from the detectors:

- DDL (Detector Data Link)
- GBT

The C-RORC FPGA has enough logic resources to implement the GBT-FPGA code in addition to the DDL code. Most of the elements of the current readout chain have been preserved in order to reduce the development time and to keep the compatibility with DATE.

The main components are:

- DDL SIU (Source Interface Unit)
- DDL DIU (Destination Interface Unit)
- RORC (Readout Receiver Card)

The SIU and the DIU provide an interface for the data transmission using the DDL protocol. The RORC performs DMA transaction to move data in the memory of the hosting PC. The SIU is located in the FEE and it sends data using the DDL protocol. The DIU is installed in the RORC, decoding the data (figure 3).

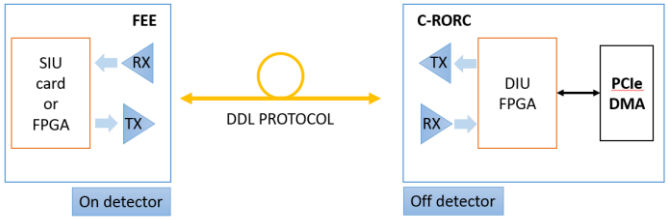

Fig. 3. ALICE DAQ readout chain, the SIU on the left communicating with the DIU on the right over the DDL.

VI. The Firmware

All the components described in the previous section are included in the new C-RORC firmware in order to read-out the GBT protocol using the present DAQ system, as shown in figure 4.

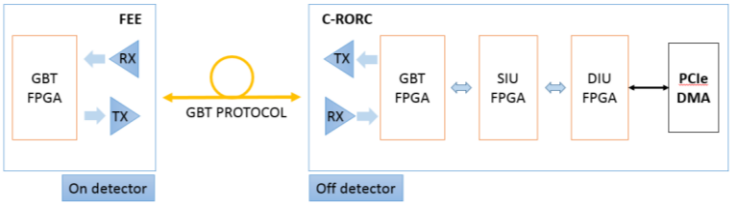

Fig. 4. The new readout chain using GBT protocol to transfer data from the FEE to the C-RORC.

The SIU-FPGA code has been ported inside the C-RORC firmware. It is directly connected to the DIU component. The GBT-FPGA is the connection point between FEE and the C-RORC. Once data is received on the GBT side it is properly formatted and delivered to the SIU. Keeping the SIU code in the C-RORC firmware allowed fast integration of the GBT with DATE. It is possible to read-out the new detector electronics without changing a single line of code. The software tools work fine without detecting the different readout protocol. The C-RORC firmware can read-out 8 GBT

links. A description of the main blocks is given in the next section.

VII. DATA TRANSFER (FEE TO C-RORC)

During RUN3 ALICE will collect data using two different readout mode:

- Triggered readout: the FEE will produce a sub-event for every trigger received. The sub-event is sent over DDL or GBT link. The detector using the GBT will insert the payload between two additional packets: Start Of Frame (SOF) and End Of Frame (EOF) packet (described in figure 5).
- Continuous readout: the FEE will produce a continuous flow of data over the GBT link. It is the responsibility of the readout card to packetize the information and to tag the data adding event identification.

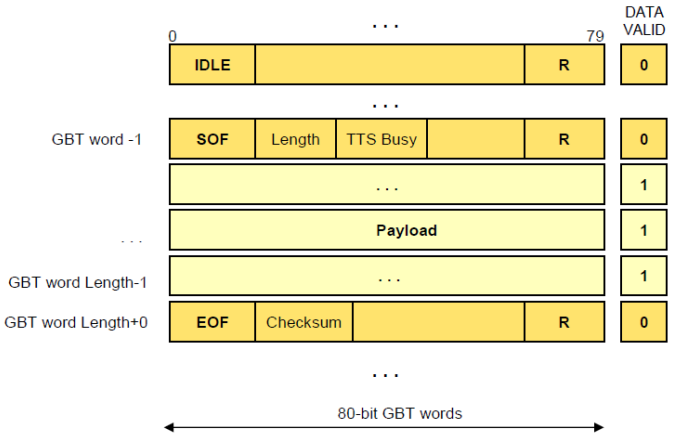

Fig. 5. GBT packetized protocol for the triggered detector.

The next sub-sections give a detailed description of all the components involved in the data transmission from the FEE to the readout card (figure 6).

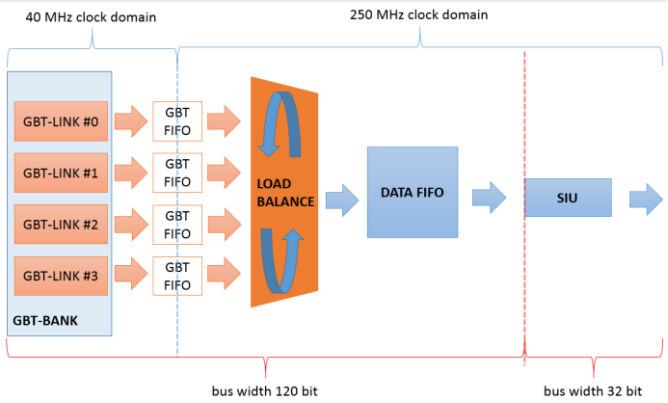

Fig. 6. The block diagram of the data flow in the C-RORC. On the left one GBT-BANK with four links and on the right one SIU interface.

A. *GBT-BANK*

The optical links are grouped in what is called *GBT-BANK*. Every bank consists of four bi-directional optical links and data can flow in both direction at the same time.

B. *GBT FIFO*

Each GBT link stores data in a small *GBT-FIFO* (120 bit x 1024 words) to buffer the data while the *LOAD BALANCE* component reads them one after the other.

C. *LOAD BALANCE*

Four input links are merged in one output port. This component is responsible to read the *GBT-FIFOs* using a round robin algorithm and to send data to the *SIU* in a single data stream.

D. *DATA FIFO*

Data in output from the *LOAD BALANCE* is stored in the *DATA-FIFO* (120 bit x 4096 words) waiting to be processed by the *SIU*.

E. *SIU*

The *SIU* reads data out from the *DATA-FIFO* and it sends the information to the rest of the chain communicating with the DIU using the DDL protocol.

VIII. SLOW CONTROL AND TRIGGER (C-RORC TO FEE)

The other available channel in the fiber, from the C-RORC to the FEE, is used to deliver triggers and upload slow control configuration to the FEE.

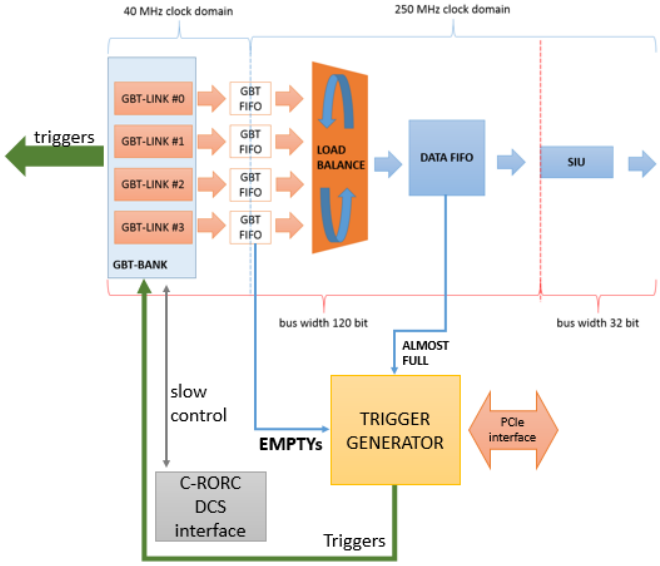

Fig. 7. The trigger generator and the DCS components connected to the GBT bank.

A. *INTERNAL TRIGGER GENERATOR*

Most of the detectors in RUN3, will receive triggers over the GBT link. The readout card must therefore receive triggers from the Central Trigger Processor and propagate them to the FEE. The C-RORC firmware implements an internal trigger generator that can be configured to function in different mode:

- *Constant frequency*: a fixed frequency is set via software (from 0 to 40 MHz).
- *BC frequency*: the triggers are generated at specific bunch crossing (trigger rate 100 KHz).
- *Heart Beat (HB) trigger*: used by continuous readout detectors. They must receive a HB trigger with specific codes during data taking, as indicated in Table 3.

TABLE 3. HEART BIT TRIGGER CODES

Trigger command	Code	Legend
SYNC	0x01	Synchronization trigger
RESET	0x02	Reset FEE
CALIBRATE	0x08	Calibration data
RESUME	0x10	Resume data taking
PAUSE	0x20	Pause data taking
EOR	0x40	Stop data taking
SOR	0x80	Start data taking

There is no BUSY concept in continuous read-out mode, it is therefore mandatory to implement some safety features in the readout chain to avoid data corruption. When the DATA-FIFO in the C-RORC reaches the almost full state, the PAUSE trigger is sent to the FEE. Once this trigger is received, the FEE sends data with no physics value (0x0) and the C-RORC can safely drop the content. Once the buffers return to a safety state, data taking can restart and a RESUME trigger is sent to the FEE.

B. *SLOW CONTROL*

The GBT fiber is the only physical connection with the FEE. The C-RORC must be able to send configuration data to the detector electronics. As described in chapter 4 the GBT packet encapsulates DCS information. Four bits in the GBT packet are reserved to send and receive slow control data.
Two of this bits are reserved to configure the GBTx chip (IC), while the other two are used by the GBT-SCA chip (EC) connected to the rest of the FEE components.

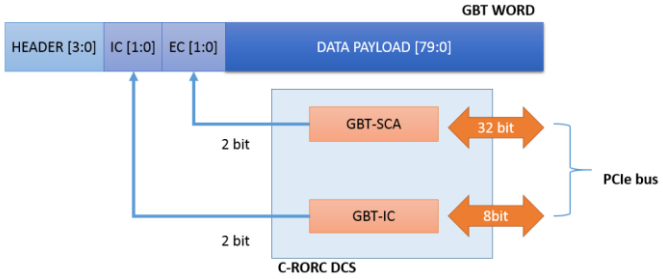

Fig. 8. The DCS user interface to send configuration data over GBT to the FEE.

The C-RORC DCS component receives in input the parallel data to be sent over GBT and it encodes the information in the 4 bits over several GBT packets.

IX. GBT DDG (DETECTOR DATA GENERATOR)

The hardware configuration of the C-RORC allows different usage and configuration of the card. A detector data generator has been built using the C-RORC hardware and developing a dedicated firmware. The C-RORC in this new configuration is used to test the readout system. This set-up is extensively used to validate the firmware when new features are developed.
The DDG supports up to 8 GBT links, each one connected to its own pattern generator, as shown in figure 10.
The DDG firmware will be upgraded following the requirements of the different detectors. It is not feasible to build a realistic test set-up using detector hardware; the DDG will be an important tool during the commissioning phase of the new readout chain. It allows to stress the read-out system with high number of links. In addition, the C-RORC hardware can be equipped with external memory. It will be possible to upload real detector data and use the DDG to send realistic simulated events over GBT.

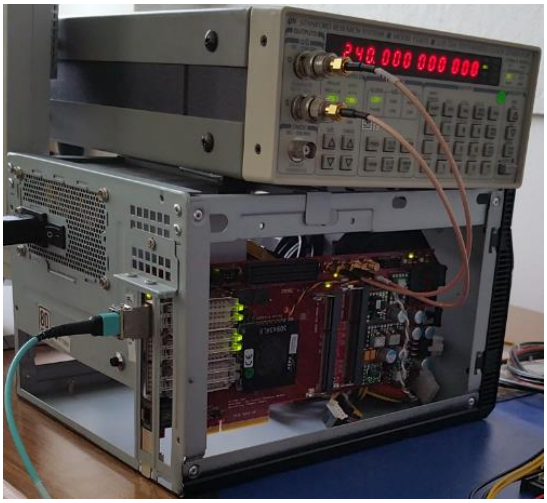

Fig. 9. The C-RORC in the DDG standalone configuration.

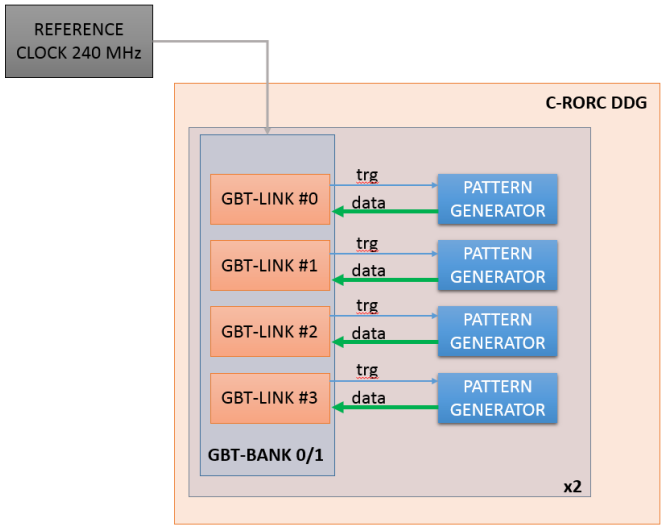

Fig. 10. DDG main firmware components

X. CONCLUSIONS

The ALICE upgrade includes a complete change of the detector read-out. A transition strategy has been established using components of the present read-out and in particular the C-RORC board. The current release of the C-RORC GBT firmware has been tested in the lab reading data from 8 GBT links in triggered mode. Tests with a real detector, the TOF, have just started. Using the TOF setup, two FEE cards equipped with an IGLOO Microsemi FPGA and a GBTx chip (figure 11), the system could run at a maximum trigger rate of 340 kHz, sending events of 1.7 kB.
This early result proves the good performance of the prototype card, fulfilling completely the requirement of TOF for RUN3 that is to be able to run with a trigger rate of 200 kHz. The plan for the future is to continue the development of the firmware in view of the future test

beams in summer 2016, extending the feature of the readout system and doing more tests with the other detectors.

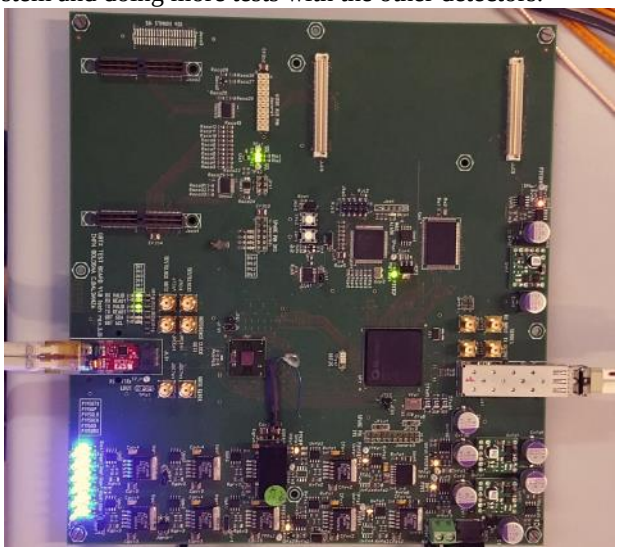

Fig. 11. TOF FEE board: on the left the GBT connection to the DAQ. In the center of the board the GBTx chip and the IGLOO FPGA from MICROSEMI.

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