An I/O Controller for Real Time Distributed Tasks in Particle Accelerators

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***Abstract*—SPES is a second generation ISOL radioactive ion beam facility in construction at the INFN National Laboratories of Legnaro (LNL). Its distributed control system embeds custom control in almost all instruments or cluster of homogeneous devices. Nevertheless, standardization is an important issue that concerns modularity and long term maintainability for a facility that has a life span of at least twenty years. In this context, the research project presented in this paper focuses on the design of a custom Input Output Controller (IOC) which acts as a local intelligent node in the distributed control network and is generic enough to perform several different tasks spanning from security and surveillance operations, beam diagnostic, data acquisition and data logging, real-time processing and trigger generation. The IOC exploits the Computer On Module (COM) Express standard that is available in different form factors and processors, fulfilling the computational power requirement of varied applications. The Intel x86_64 architecture makes software development straightforward, easing the portability. The result is a custom motherboard with several application specific features and generic PC functionalities. The design is modular to a certain extent, thanks to an hardware abstraction layer and allows the development of soft and hard real-time applications by means of a real-time Operating System and the on-board FPGA closely coupled to the CPU. Three PCIe slots, a FPGA Mezzanine Card (FMC) connector and several general-purpose digital/analog inputs/outputs enable functionality extensions. An optical fiber link connected to the FPGA is an high speed interface for high throughput data acquisitions or time-sensitive applications. The power distribution complies the AT standard and the whole board can be powered via Power Over Ethernet (POE+) IEEE 802.3at standard. Networking and device-to-cloud connectivity are guaranteed by a gigabit Ethernet link. The design, performance of the prototypes and intended usage will be presented.**

I. Introduction

THE Control System is a key component for the operation of the accelerators complex at the Laboratori Nazionali di Legnaro (LNL) [1]. In this context, the development of the SPES facility [2] comes together with an important campaign for hardware and software standardization and upgrade. Part of the SPES facility is completely new, while, for the rest the SPES project will exploit the ALPI accelerator for accelerating radioactive ion beams. The idea behind the new IOC is to integrate subsystems having different levels of complexity and real-time requirements to an homogeneous architecture. EPICS [3] was chosen as control system framework for collecting distributed data in the new environment. From the hardware point of view, the standardization is achieved by the custom IOC, which is the subject of this paper. The IOC aims to be an universal controller capable of extending the control reach to all the equipment in a complex facility. It will be embedded into physical equipments and will control or monitor their operation allowing the computational load to be spread among intelligent nodes in the control network. The IOC is centered around the COM Express module [4] and a Xilinx Spartan 6 FPGA leaving the final user with the possibility to deal with a general purpose PC with a good level of hardware functionality abstraction or to exploit the FPGA in terms of fast peripherals control, thus freeing operating system from hard real-time tasks. Time-sensitive operations such as synchronous messaging or data alignment are ordinary in physical experiment facilities. Timing requirements may be so strict as become unfeasible via software; hardware enhancements are essential and have been considered in the IOC design. The acquired data may be elaborated locally ensuring the generation of a feedback within a bounded amount of time, or, data from each IOC may be shared on the network in case of slow control remotely performed tasks. The beam diagnostic system of SPES, described hereby following, it exploits the IOC for executing many independent, time-critical, and parallel tasks.

II. Hardware Architecture and Main Features

This chapter takes the reader through the main IOC features. The COM Express guidelines [5] have been the main reference to endow the IOC with general purpose PC features. As shown in Fig.1, all generic PC functionalities are readily available in an off-the-shelf module along with more system specific features related to the on-board FPGA.

The block diagram provides an overview about the on-board peripherals and their mapping to the central processor or to the FPGA respectively. IOC must cover all the needs for the current and future control systems at LNL.

A. COM Express

The COM Express is available in three different form factors:

- Basic

978-1-5090-2014-0/16$31.00

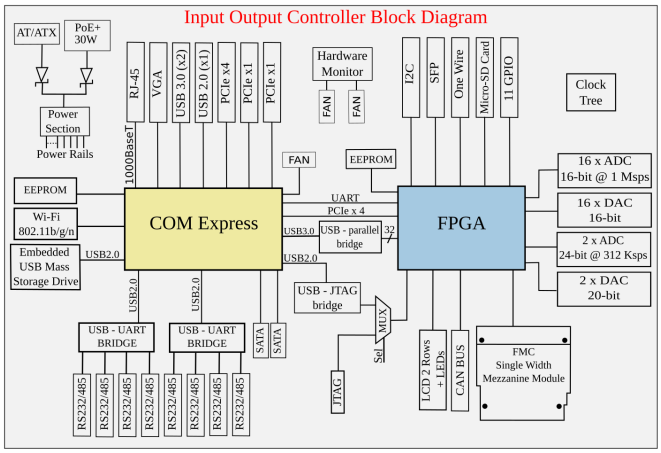

Fig. 1. IOC Block Diagram.

- Compact
- Mini

IOC has been designed to accommodate all these sizes. Each of these form factors support different processors satisfying specific level of processing performances. As one of the key feature of the IOC is to be Power Over Ethernet Plus (PoE+) compliant (PoE+ standard [6] foresees power distribution on the Ethernet network for a maximum of 26 W). We plan to use the compact form factor together with the low power Intel Atom quad-core processor shown in Fig.2.

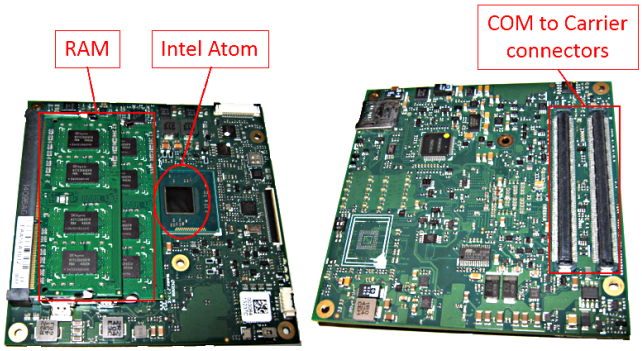

Fig. 2. cExpress-BT Intel Atom E3845 @ 1.91 GHz.

B. Boot Options

The goal is to use in all our applications a standard Linux distribution; the most time-critical tasks will run in the FPGA avoiding the need of a real-time operating system. Following are the main boot options supported by the IOC:

- Two SATA-150 connectors to be able to boot from an external Solid State Drive (SSD).
- Embedded USB 2.0 Mass Storage Drive. This tiny NAND flash memory, shown in Fig.3, is foreseen for embedded applications requiring a custom minimal operating system. We successfully booted a standard Linux distribution.
- Network booting.

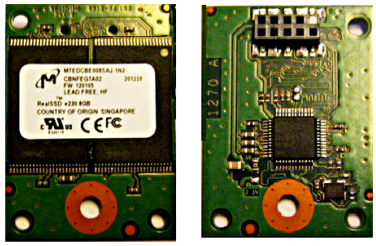

Fig. 3. Micron Embedded USB Mass Storage Drive.

- Micro-SD card. See Fig.2.
- Any USB bootable flash drive.

C. Network Connectivity

Device to device and device to cloud connectivity are of primary importance for an embedded controller. The control system at LNL is distributed on an Ethernet network and therefore the preferred interface is the LAN port. This 10/100/1000BaseT gigabit Ethernet interface complies to the IEEE 802.3-2005 standard. Both the PHY and MAC layers are integrated in the COM Express module thus the carrier hosts only the PoE+ section. Where galvanic isolation is needed (as in high-voltage applications) the IOC provides a Wi-Fi interface and an optical fiber interface directly linked to the FPGA. Fig.4 shows the Wi-Fi module integrated in the IOC that supports IEEE 802.11b/g/n standards. The chip communicates with the COM Express host via a Standard Peripheral Interface (SPI) port and the maximum data throughput achievable is 12 Mbps.

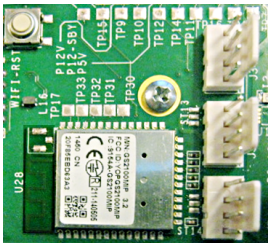

Fig. 4. WiFi GS2100MIP.

The optical link may be used to send and receive synchronous messages, or to implement high speed data transfers between logical units whenever Ethernet protocol does not match the given time constraints, or to implement an optical Ethernet interface. The IOC has been designed to provide the processor with an Ethernet interface through the optical link [7]. A block diagram is shown in Fig.5 where the Physical Coding Sublayer (PCS), either Ethernet or PCIe, is done in the FPGA.

D. FPGA and Hard Real-Time Tasks

FPGAs are vastly used in custom embedded systems due to their high degree of modularity and the fast peripherals control required in real-time systems. The idea underlying the IOC is to fully exploit the potential of both the processor and the FPGA as two separate units: the COM Express and a Xilinx

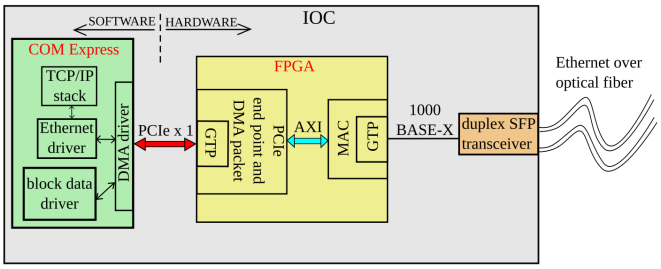

Fig. 5. Optical Ethernet Block Diagram.

Spartan-6 XC6SLX75T. This makes the design modular and the application development and portability straightforward. Any Linux or Windows application can run out of the box without major reworks. The carrier power distribution has been designed such that the power rails related to the FPGA and its peripherals are completely independent from the power rails supplying the COM Express and the general PC interfaces. Hence FPGA and COM Express can be used as independent units (also mutually exclusive), or, strictly coupled as most of applications at LNL require. The communication between these two units is ensured via three different links:

- UART. Simple and low cost solution to provide slow control communication.
- PCIe 1.0 x 4 link.
- USB 3.0 to 32 bits parallel bus bridge based on Cypress CYUSB3014.

The VHDL core that handles the communication with the COM Express allows a transparent map of the FPGA registers and I/O resources into the I/O space of the PC. In this way the resources linked to the FPGA become virtually part of the COM Express memory.

E. Remote Device Configuration and ChipScope

FPGA remote reconfiguration is of primary importance for applications where accessibility is a concern after installation on the field. Firmware may get corrupted during the reconfiguration phase itself and also stall situations due to bugs in the firmware may occur. Therefore it is advisable to access the JTAG chain and re-flash the FPGA via the Ethernet network. Fig.6 resumes how this is done in the IOC.

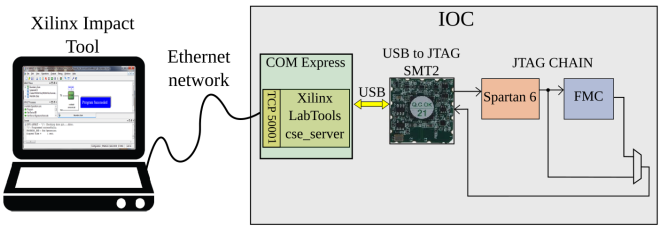

Fig. 6. FPGA Remote Configuration.

A mix of software servers in the COM Express module and an hardware bridge (USB to JTAG) in the carrier side allow remote reconfiguration of the on-board FPGA as well as the complete availability of debug tools [8] for FPGA design commissioning.

F. Analog I/O Channels

The IOC embeds several analog I/O channels to ease integration on the field. Data conversion at LNL falls into two different categories:

1) data acquisition for real-time control and processing;
2) data acquisition for data storage.

Depending on the required feedback latency, the acquired data can be elaborated locally by the FPGA or by the processor, or remotely in a central server (slow control applications). IOC integrates several I/O analog channels:

1) 8 dual ADCs AD7903, 16-bit @ 1 Msps, input voltage range $\pm$ 10 V;
2) 2 ADCs AD7764, 24-bit @ 312 Ksps, input voltage range $\pm$ 10 V;
3) 8 dual DACs AD5752, 16-bit, output voltage range $\pm$ 10 V;
4) 2 DACs AD5791, 20-bit, output voltage range $\pm$ 10 V.

The dynamic range and sample rate can be complemented with commercial solutions in FMC or PCIe form factor. Previous works [9] based on commercial PCIe ADC boards have shown that by scanning the input channels via software, the CPU usage increases dramatically with the sample rate, that is therefore limited to a few Ksps. The FPGA gets around this limitation and allows the user to take advantage of the full ADCs bandwidth.

III. PCB Development

The place and route of the board has demanded some time due to the design complexity. Fig.7 shows the design flowchart which has been followed.

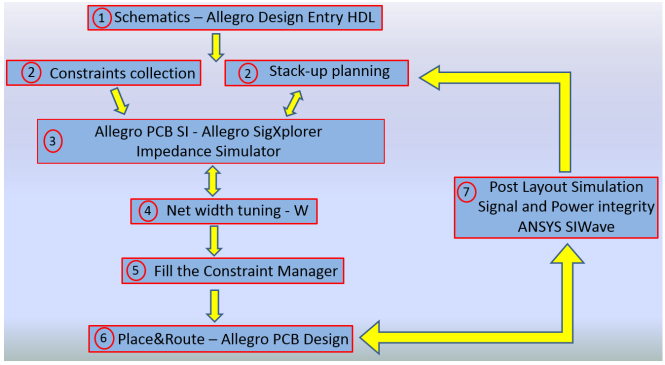

Fig. 7. PCB Design Flowchart.

We have designed a 14 layers stack-up based on Isola FR408HR dielectric to ensure adequate performance. The grounding strategy has been analyzed carefully since the beginning due to the presence of PoE+ powering together with high resolution analog converters. The PCB layout has been extensively validated by means of power and signal integrity simulators and with lab tests on the prototypes. Fig.8 underlines the layout complexity. Only signal layers are shown.

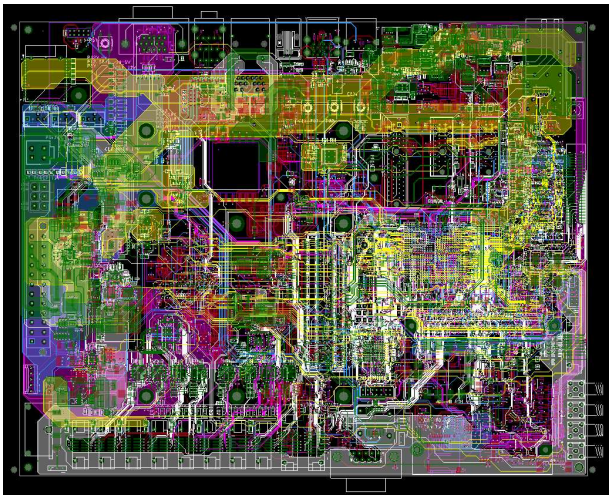

Fig. 8. IOC layout - Signal Layers.

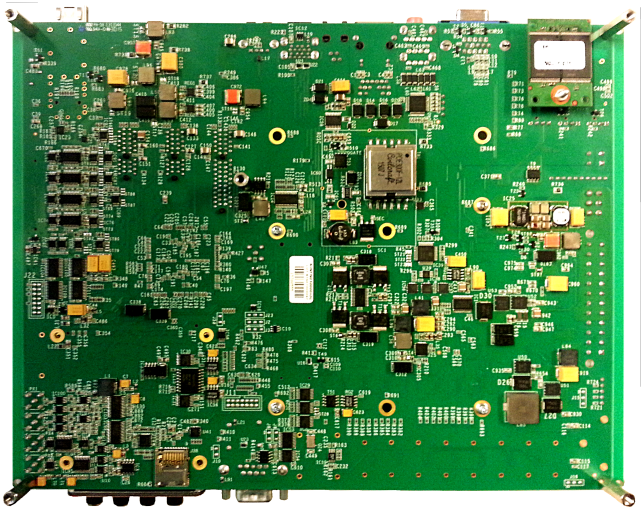

Fig. 10. Input Output Controller Bottom View.

IV. IOC Status

IOC is in advanced prototyping stage. Two prototypes have been built and the main features have been tested. Fig.9 and Fig.10 show the IOC top and bottom views respectively.

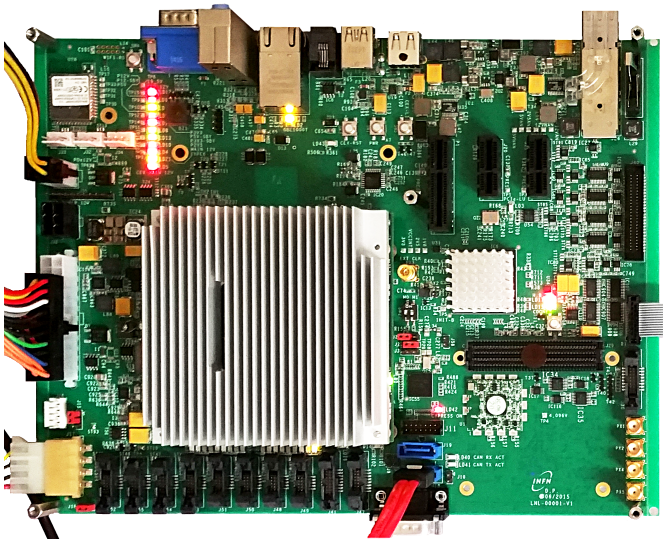

Fig. 9. Input Output Controller Top View.

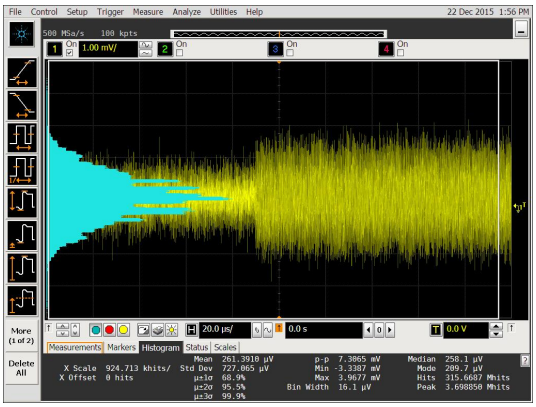

Fig. 11. FPGA Core Power Supply Noise Measurement.

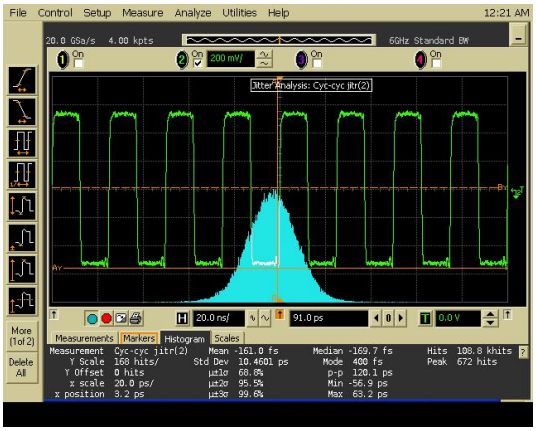

Fig. 12. Cycle-to-Cycle Jitter Analysis. The Std Dev achieved is 10.46 ps. The target value is 50 ps.

Ripple measurements have been carried out on the power rails; a lack of power integrity may compromise the overall performance. Fig.11 shows the FPGA core voltage supply; the voltage ripple achieved is 7.3 mV p-p @ 727 uV rms.

The clock tree has been validated through an accurate jitter analysis as shown in Fig.12

The COM Express module used is cExpress-BT with an Intel Atom E3845 processor running a standard Linux Distribution (Ubuntu 14.04). We tested all the PC peripherals (VGA, USB 2.0, USB 3.0, SATA, gigabit Ethernet, PCIe), while other specific features have been tested with custom developed local software. The eight RS232/RS422 transceivers directly linked to the processor have been integrated in the linac magnet control system thanks to the EPICS framework. We are currently developing the firmware (VHDL) for debugging the FPGA connected peripherals. The first production version is foreseen before the end of the current year.

A. Analog Input Channel Test

We focused on Signal to Noise and Distortion Ratio (SINAD) and Effective Number of Bits (ENOB) as indicators of the overall performance of the analog channels as found on literature [10]. Fig.13 shows the ADC test setup.

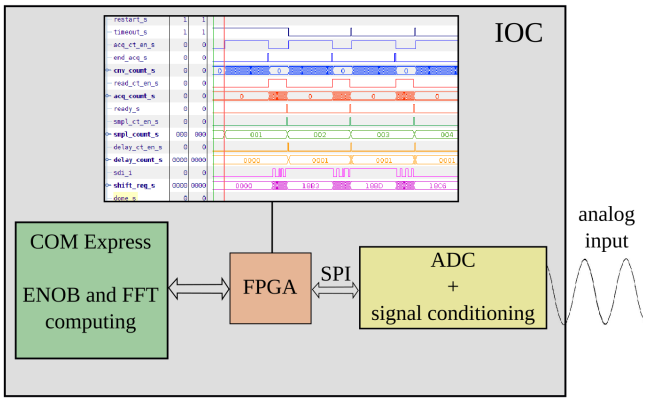

Fig. 13. ADC Test Setup.

Ideally, one has to feed the analog input with an ideal sine-wave. In order to account for the contribution of the waveform generator to the total harmonic distortion, we have adopted the following policy for analog channel testing. First, we have sampled the analog noise floor by shortening the ADC input to ground. Then, a Matlab ® generated harmonic with normally distribute quantization noise has been added to the sampled noise floor and the SINAD has been computed. Finally, ENOB can be computed using the following relation:

$$ENOB = \frac{SINAD - 1.76 + 20\log\frac{FullscaleAmplitude}{InputAmplitude}}{6.02}$$

ENOB measurements have been performed for all the analog input channels. Some examples are provided here below. Fig.14 shows the ENOB achieved with the 16-bit resolution analog input channels and a sampling frequency of $948\,\mathrm{Ksps}$.

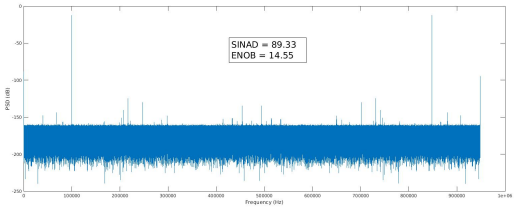

Fig. 14. ENOB ADC 16-bit = 14.54.

Our measurements are in good accordance with the component specification reporting a maximum ENOB of about 15 when the reference voltage is set to $4\,\mathrm{V}$. Fig.15 reports the Power Spectral Density (PSD) achieved with the 24-bit ADC together with the sine wave tone set to 95 percent of the voltage input range. The sampling frequency was set to $312\,\mathrm{Ksps}$ (maximum) whereas the sinusoidal tone frequency is $100\,\mathrm{KHz}$.

The ENOB upper limit deduced from the data sheet of the component is 17.8 and it is basically limited by the maximum

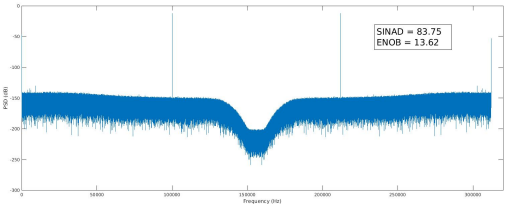

Fig. 15. ENOB ADC 24-bit = 13.62.

Signal to Noise (SNR) ratio achievable in the PCB. In all our measurements we tried to reproduce the worst noise conditions and more tests will be performed to investigate and enhance the ENOB of the 24-bit resolution channels. The PSD plot gives us important information on the ADC bandwidth; the Sigma Delta architecture exploited to achieve high resolution has an internal digital low pass filter with selectable corner frequency. The low pass behavior is well visible at $150\,\mathrm{KHz}$ and we expect a reduction of ENOB moving the sine tone close to the Nyquist frequency.

V. Application of IOC in the Beam Diagnostic System

The IOC debug phase is carried out alongside tests on the field. We aim to use the IOC in several different applications and the beam diagnostic system is reported here as a typical use case. The diagnostic system provides information on the beam transverse profile and energy and on the time and spatial distribution of particle bunches. An upgrade campaign of the existing ALPI beam diagnostic system is being carried out. The main upgrades are related to the electronics readout system and the software integration [11] of the diagnostic boxes in the LNL control system. One of the beam diagnostic devices is the Beam Profiler Monitor (BPM) shown in Fig.16. It consists of a grid of thin wires (twenty horizontal and twenty vertical) made of gold plated tungsten ($50\,\mathrm{um}$ diameter) injected and extracted in/from the beam line through stepper motors. The ion beam crossing the grid deposits a charge on the wires. Only a small percentage of the beam current is caught by the wires depending on the wires diameter and spacing.

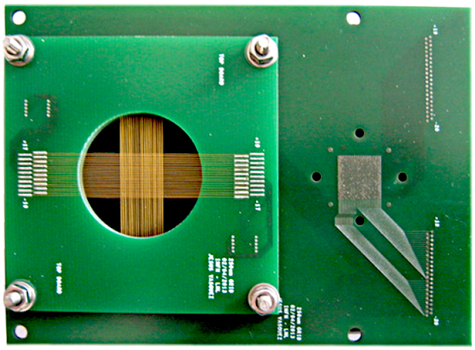

Fig. 16. Beam Profiler Monitor.

The beam profiler must be able to reconstruct the beam transverse profile by reading out the current from each wire.

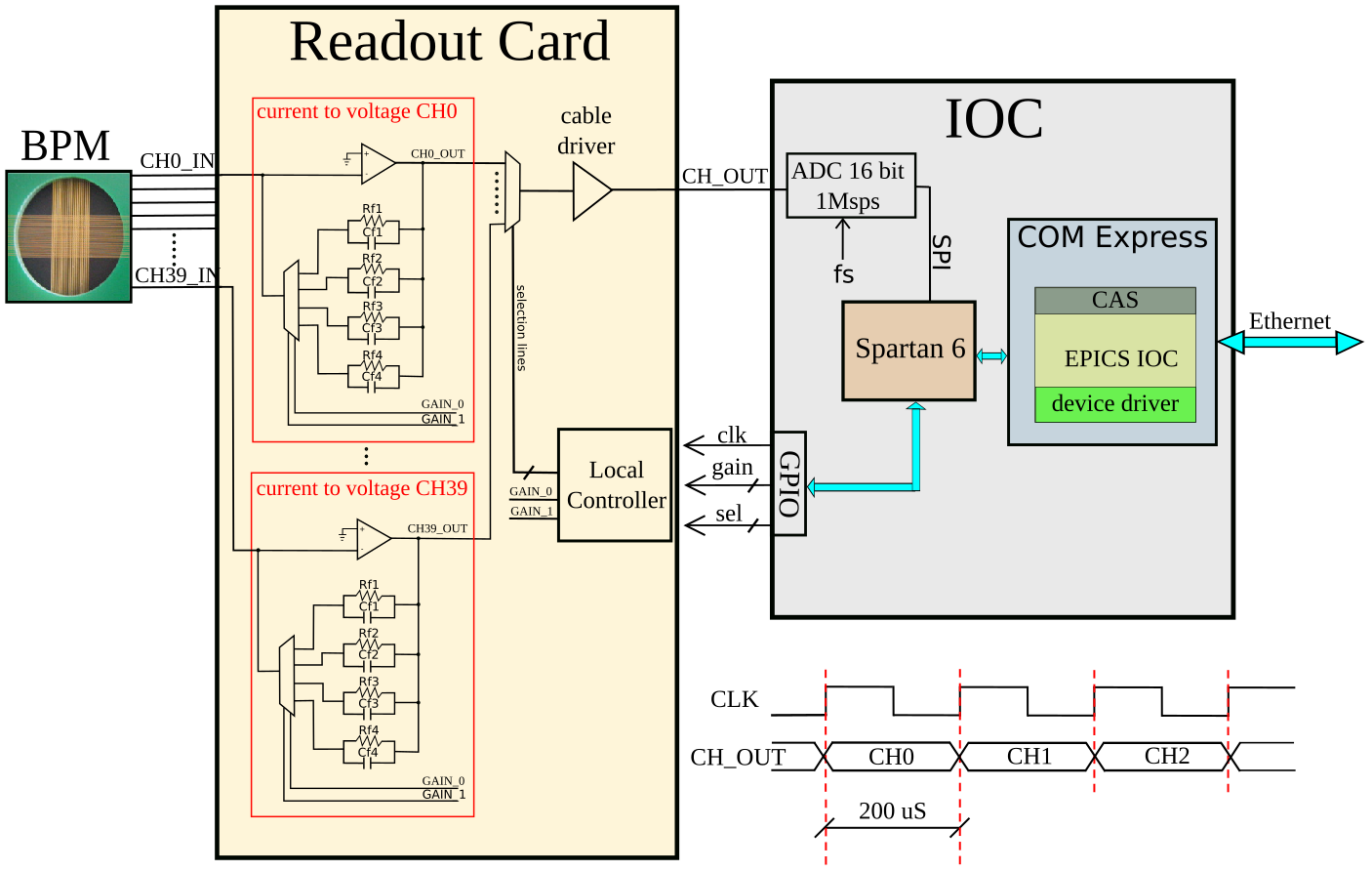

Fig. 17. BPM Data Acquisition Architecture.

The existing acquisition system [12] is based on a current to voltage and pre-amplifier card, a VME ADC board for the digitization driven by a VME CPU board which sends the acquired data to the remote control room via Ethernet for the beam profiles visualization. The logic card controlling the data acquisition system must run several parallel tasks, some of them have time-critical requirements. The present system foresees the usage of VxWorks real-time operating system to match these time requirements. The new BPM data acquisition system architecture will be based on the IOC and the most time-critical tasks are performed in the FPGA freeing the CPU from hard real-time operations. The legacy VME crate together with the ADC card and the CPU card will be replaced by a single IOC. VxWorks operating system can be replaced by an open source operating system like Linux. Fig.17 shows the new BPM data acquisition architecture which is being developed. The grid's front-end electronics is composed of the readout card, placed in the proximity of the diagnostic box, that hosts 40 current to voltage converters, together with a multiplexer and a cable driver. The 40 channels are multiplexed to a single voltage analog output and then sampled by an analog input channel in the IOC that provides also the digital control output signals. Since BPM must accommodate different beam intensities it is mandatory to be able to set the pre-amplifier gain accordingly. The readout card current sensitivity extends from a few pA to hundreds of nA. The integrator time constant is so given:

$$\tau = R_f C_f$$

and in all gain settings it is about 100 ms, well above the bunches period (12.5 ns). The scanning of the forty channels is controlled by the clock signal coming from the IOC and lasts 40 x 200 us period pulses. The generation of the pulses together with the synchronized gain and selection signals, which was a concern in the previous architectures (scanning done via software), now, it can be even easily done in hardware via the FPGA. The FPGA firmware handles also the ADC conversion, data buffering and Direct Memory Access (DMA) data transfers to the processor. COM Express implements an EPICS Channel Access Server (CAS) making BPM data available to remote EPICS clients for display visualization. Supposing a refresh rate of about 20 frames per second, the total data throughput is 2.56 Mbps considering 16-bit resolution and 1 Msps as sample rate (worst case). This data rate is well in the range of the gigabit Ethernet. EPICS will also integrate in the control system the slow controls for stepper motors.

VI. Conclusion

A custom Input Output Controller has been designed and tested. The on-board peripherals address the needs of most control subsystems at LNL. IOC allows for hardware standardization and will replace legacy hardware with cutting-edge

technologies embedded in the custom mother board. It matches with the distribute control system architecture foreseen by EPICS, preserving the possibility to manage distribute hard real-time tasks. Beam diagnostic data acquisition, electrostatic beam focalization and extraction, magnetic and electrostatic beam steerers are target applications and ideal test benches for the developed IOC.

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