New LLRF Control System at LNL

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Abstract

The Low-level Radio Frequency (LLRF) control system for linear accelerator at Legnaro National Laboratories (LNL) of INFN is being upgraded by a new digital Radio Frequency (RF) controller. This controller is critical to keep phase, amplitude and frequency stability of the RF field in Quarter Wave Resonator (QWR) cavities of the linear accelerator. These cavities work in superconducting condition. The resonance frequency of low beta cavities is 80 MHz, while medium and high beta cavities resonate at 160 MHz. Each RF controller can control at the same time eight different cavities. The RF signals picked-up from the cavities are sampled by RF ADCs. The digitized signals are fed into a field programmable gate array (FPGA) which implements the control loop. The signals processed by the FPGA are in-phase/quadrature modulated and sent to power amplifiers and hence to the cavities. The main feature of the new control system is an all-digital control loop that originates from direct sampling of the antenna RF signal. In-phase and quadrature components are obtained by a suitable choice of the undersampling frequency, while control of the field and phase in the cavity is based on a digital Complex Phase Modulator (CPM). This paper presents the FPGA firmware, the acquisition techniques and the performances of the new RF controller.

RF system

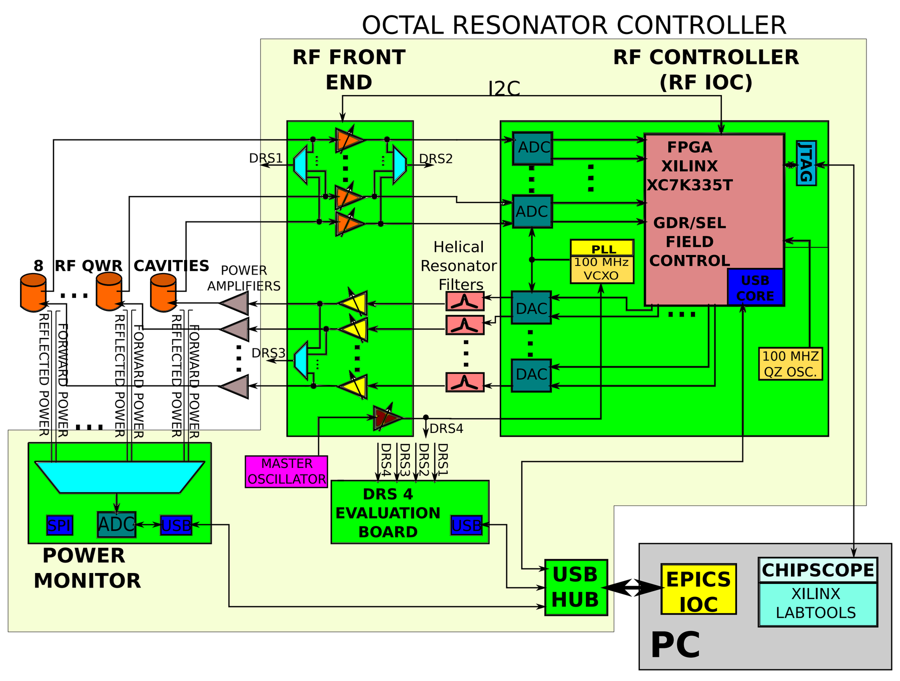

Figure 1: Block Schema of the Rack.

Figure 2: Setup used for field test of the new RF control system. The rack contains a personal computer (PC) and the octal resonator controller (OCR).

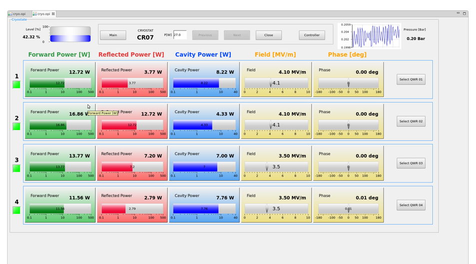

Figure 3: CSS Interface for monitoring the working status of a cryostat.

OCR essentially contains a RF I/O controller card (RF IOC), a RF front end board (RFFE), a Power Monitor board (PM), two DRS evaluation boards, an USB hub and eight Helical Resonator filters.

RF IOC

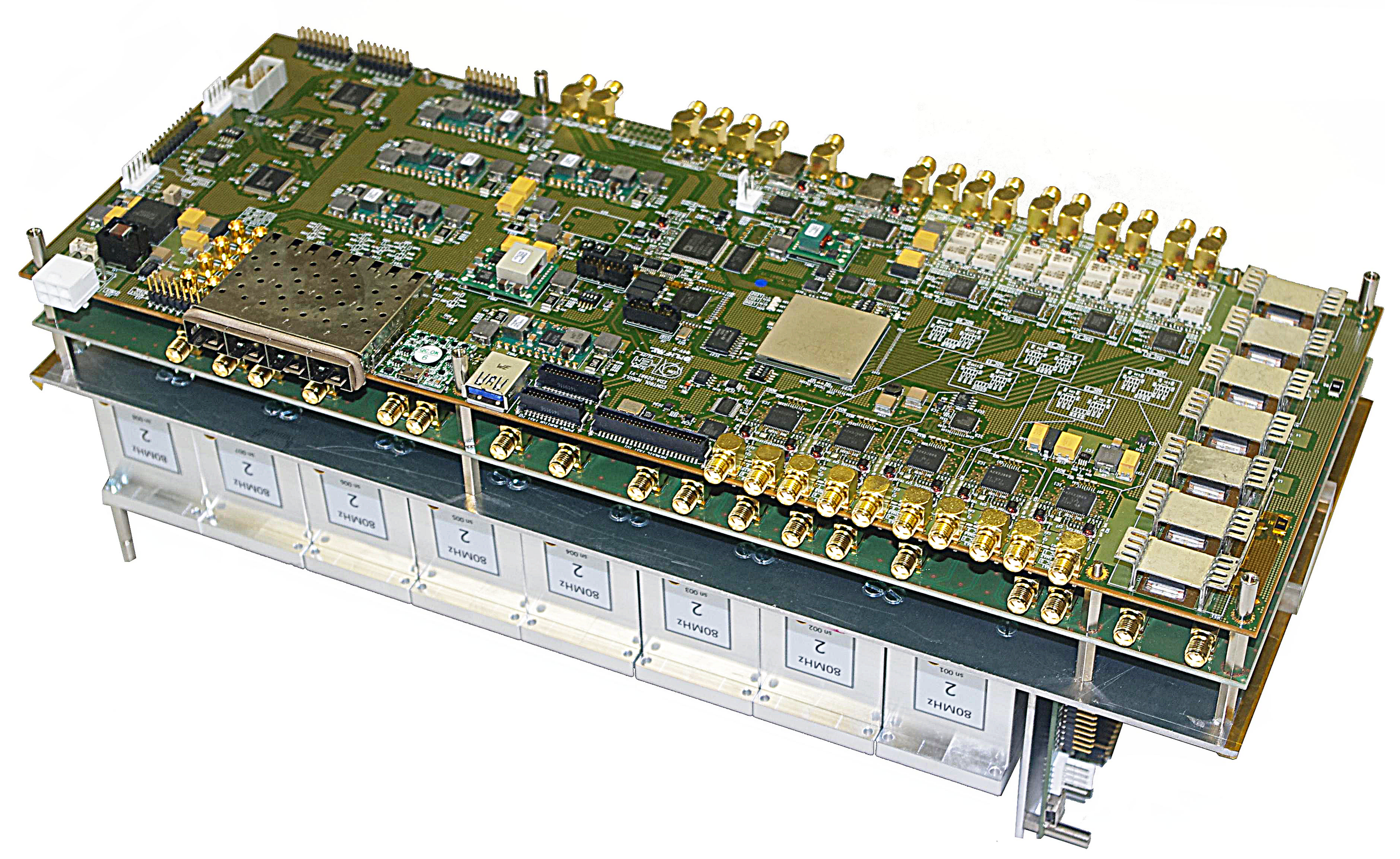

Figure 4: RF I/O controller (RF IOC) on first floor.

The RF IOC is composed of RF ADCs for the direct sampling of the signals attenuated/amplified picked up from cavities, a Xilinx Kintek 7 FPGA for signal processing (Fig. 5) and RF DACs for driving power amplifiers and hence the cavities.

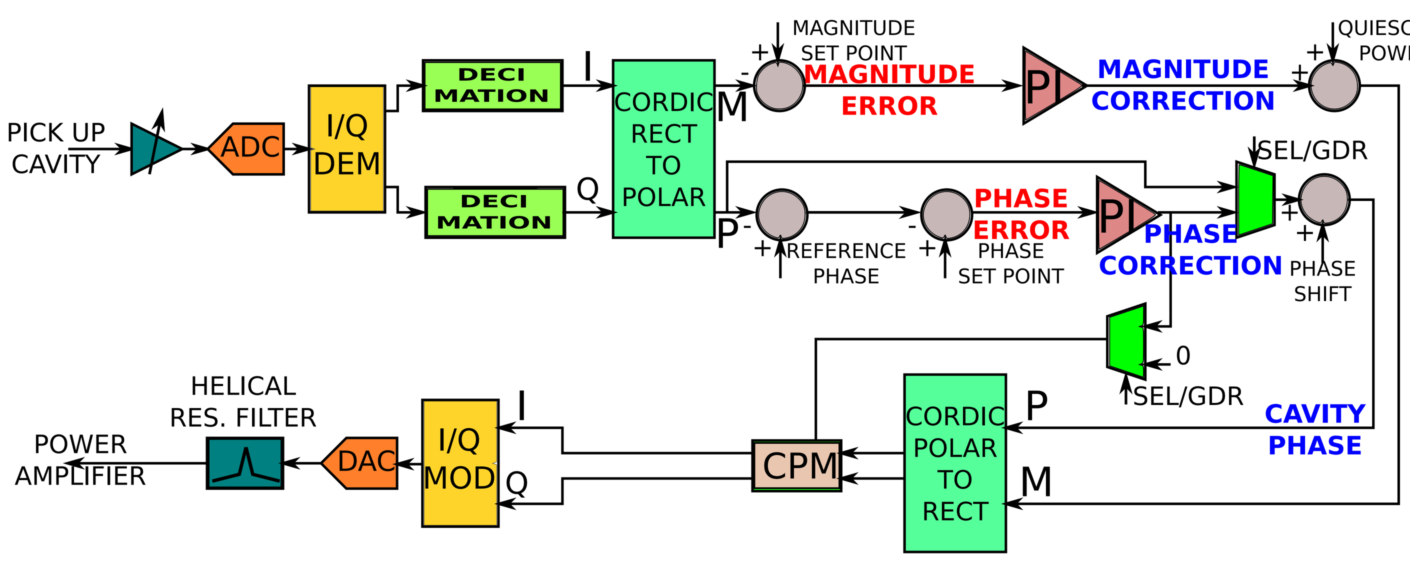

Figure 5: FPGA Data Flow.

Measurements and Results

The RF I/O controller board hosts 16-bit, 250 MSPS ADCs. The maximum Nyquist frequency available with these ADCs is smaller than the RF frequencies of interest, so **under-sampling** is adopted.

In order to extract the I/Q information, the sampling frequency f_s has to be chosen following:

$$f_{RF} = \frac{1}{D}\left(kf_s \pm \frac{f_s}{4}\right), \forall k \in Z | k \geq 1 \tag{1}$$

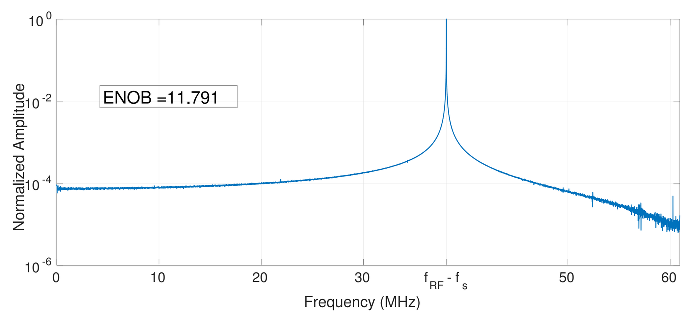

Figure 6: Theoretical ENOB @ 160 MHz

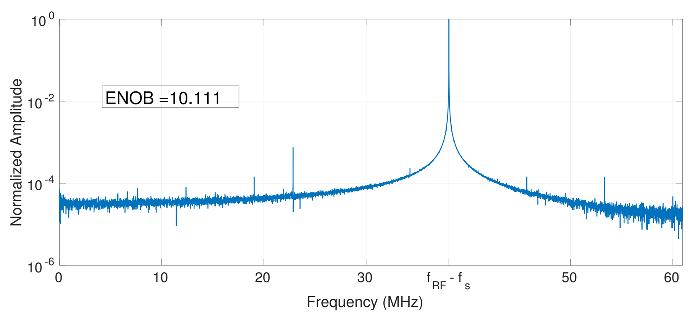

Figure 7: Actual ENOB @ 160 MHz

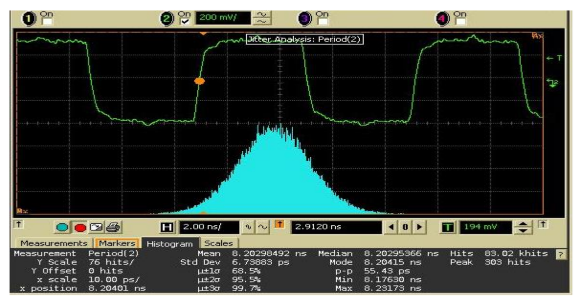

Figure 8: Clock signal of the ADCs

In RF sampling ADC, clock and aperture jitter have large impact on the resulting error. To reduce the impact a moving average of subsequent samples is implemented in FPGA.

The drift of the phase signal at the output of the first CORDIC block versus the temperature was evaluated. A value of $-0.22°/°C$ was found.

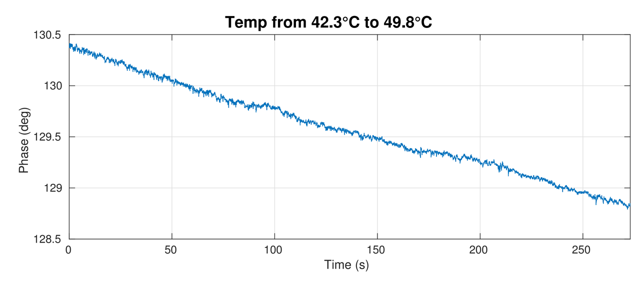

Figure 9: Phase drift in time when the temperature measured in the RF IOC changes from 42.3 °C to 49.8 °C.

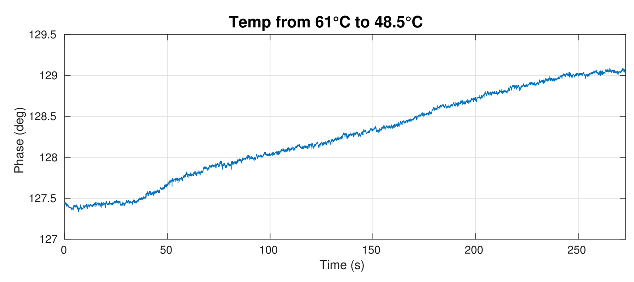

Figure 10: Phase drift in time when the temperature measured in the RF IOC changes from 61.0 °C to 48.5 °C.

The phase and magnitude stability were evaluated with an accelerated beam current of few nA of ^{32}S and eight phase and amplitude locked cavities. In the course of the testing sessions, the magnitude and phase loops were locked in SEL mode. The next figures show the phase and magnitude error during SEL operation for a medium beta cavity. The phase error is $0.011°$ rms and the total relative magnitude error is $1.54 \cdot 10^{-4}$ rms.

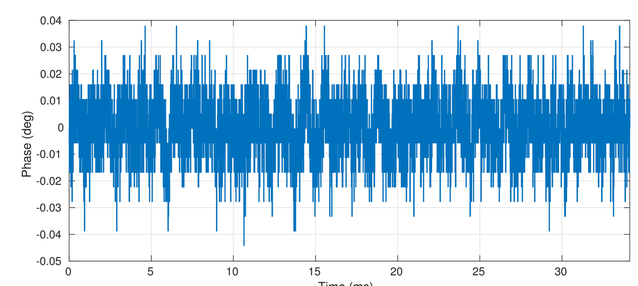

Figure 11: Phase Error for a medium beta cavity running in SEL mode.

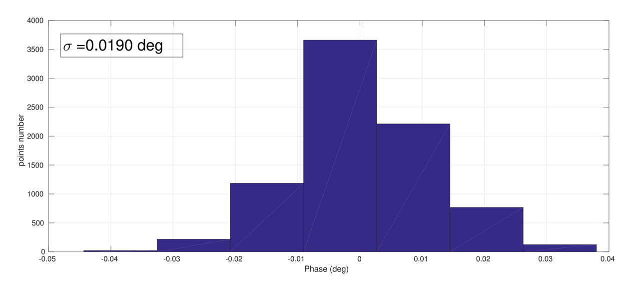

Figure 12: Distribution of the Phase Error for a medium beta cavity running in SEL mode.

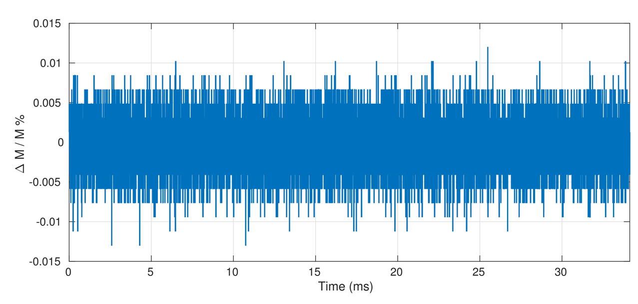

Figure 13: Relative Field Error for a medium beta cavity running in SEL mode.

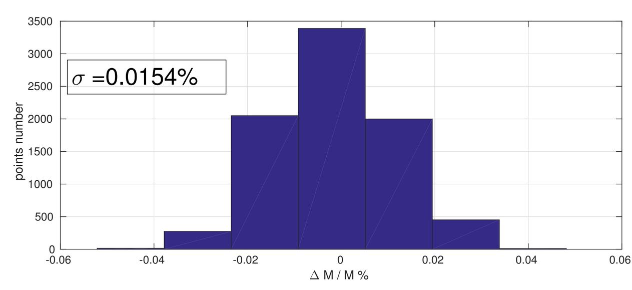

Figure 14: Distribution of the Relative Field Error for a medium beta cavity running in SEL mode.

The tests on the robustness of the feedback control loops, in phase and in amplitude are reported in the next figures. These were done studying the transient response of the RF field in the cavity changing the set-points in amplitude and phase.

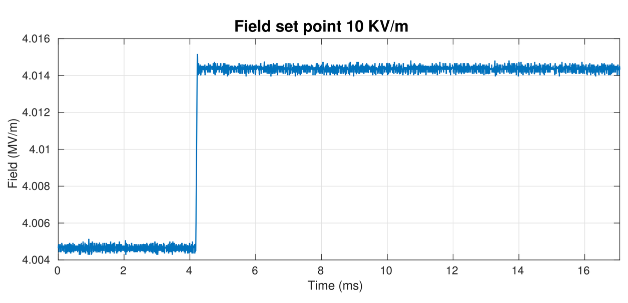

Figure 15: Step response of the field magnitude for a medium beta cavity.

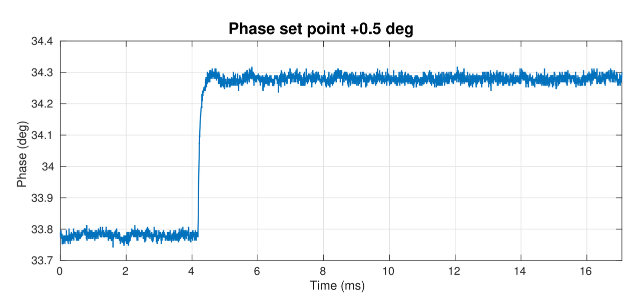

Figure 16: Step response of the phase for a medium beta cavity.

Conclusions

- **The controller has proven to respect phase and gradient field stability requirements**;
- A temperature dependency has come into evidence with the Low-Level Radio Frequency (LLRF) system;
- An excessive clock jitter of 55.4 ps p-p has been measured in the controller board. It is advisable to reduce the jitter with a careful clock distribution network on the printed circuit board.

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