New LLRF Control System at LNL

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***Abstract*—The Low-level Radio Frequency (LLRF) control system for linear accelerator at Legnaro National Laboratories (LNL) of INFN is being upgraded by a new digital Radio Frequency (RF) controller. This controller is critical to keep phase, amplitude and frequency stability of the RF field in Quarter Wave Resonator (QWR) cavities of the linear accelerator. These cavities work in superconducting condition. The resonance frequency of low beta cavities is 80 MHz, while medium and high beta cavities resonate at 160 MHz. Each RF controller can control at the same time eight different cavities. The RF signals picked-up from the cavities are sampled by RF ADCs. The digitized signals are fed into a field programmable gate array (FPGA) which implements the control loop. The signals processed by the FPGA are in-phase/quadrature modulated and sent to power amplifiers and hence to the cavities. The main feature of the new control system is an all-digital control loop that originates from direct sampling of the antenna RF signal. In-phase and quadrature components are obtained by a suitable choice of the undersampling frequency, while control of the field and phase in the cavity is based on a digital Complex Phase Modulator (CPM). This paper presents the FPGA firmware, the acquisition techniques and the performances of the new RF controller.**

***Index Terms*—Direct under-sampling, ENOB, EPICS, FPGA, linear accelerator, low level radio frequency (LLRF) controller, step response, Radioactive Ion Beam (RIB) facility.**

I. Introduction

THE linear accelerator ALPI [1] (which stands for Acceleratore Lineare Per Ioni) Fig.1, can boost the beam coming from the Tandem XTU accelerator, but also from a second and smaller linac, called PIAVE (acronym for "Positive Ion Accelerator for Very Low velocity ions"). ALPI linac consists in 96 cavities QWR type, operating in superconducting conditions. The ALPI cavities are housed in helium refrigerated cryostats. Ion bunches cross, in the region where electric field is highest, the QWR cavity and they are accelerated by the two gaps between the central drift tube electrode and the surrounding cylinder cavity. The resonance frequency of a first group of ALPI cavities is 80 MHz, while that of a second group is 160 MHz.

The LLRF control system plays an important role in modem accelerators. By stabilizing the phase, the amplitude and the frequency of RF field cavity, this system ensures an optimum energy gain of the accelerated beam. Hence the accelerating gradient and the phase stability has to respect tight requirements. In general it is required a phase stability from 0.1° to 0.5° and a gradient stability from 0.005% to 0.05% rms [2].

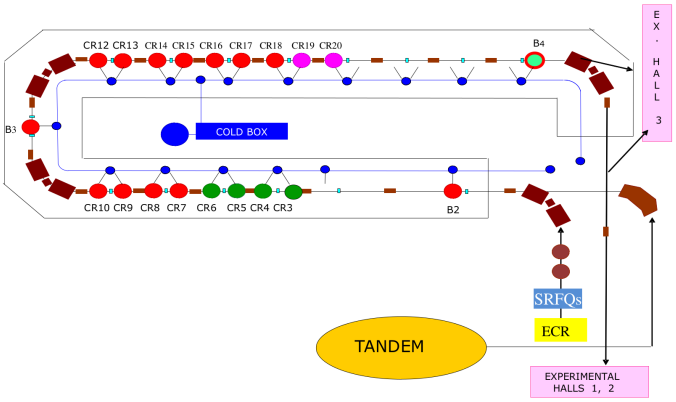

Fig. 1. Layout of ALPI

The cavities act as filters, with an extremely high quality factor Q, due to their superconducting nature. They have a narrow frequency bandwidth and their capacity to store energy decreases rapidly outside the resonance frequency. The power necessary to keep a certain RF field outside the resonance condition is consequently high. It is then essential to extend the frequency range to compensate small perturbations. The main perturbations are caused by microphonics, having frequencies from a few Hz up to some kHz. The principal sources of perturbation are pressure variation in the helium bath, temperature, mechanical vibrations, presence of currents/charges inside the cavity which influence the cavity resonance frequency in time ranges of seconds and minutes. These perturbations have to be compensated by the low-level RF control system.

II. Control system

The present RF control system was developed at LNL at the beginning of nineties [3]. It is actually used, but there is the need to improve phase and amplitude stability and resolution. In order to cope with the new Radioactive Ion Beam (RIB) facility that is in construction now at the site, a new digital RF controller system has been designed, based on direct sampling of RF signal and digital processing based on FGPA. This allows a greater flexibility in programming, and diagnostic capabilities, since it is possible to monitor many signals during the processing of the data inside the FPGA, like magnitude

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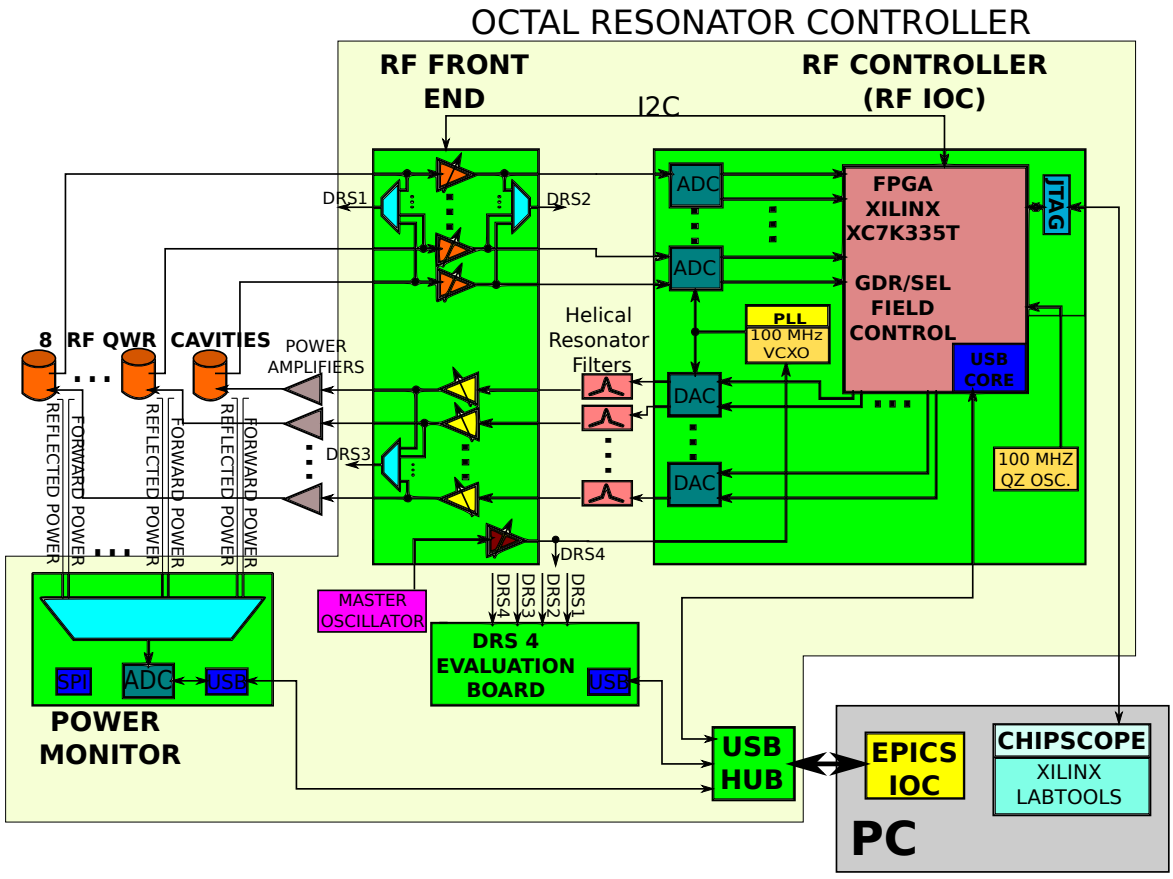


Fig. 2. Block Schema of the rack containing the octal cavities resonator (OCR) and the PC

field and phase in cavities, magnitude and phase errors. Moreover there is the possibility to choose the excitation mode of each single cavity. Besides the commissioning of the new RF controller, the control system of the linear accelerator has also been upgraded. The framework chosen for this task and for the other subsystems of the accelerator is EPICS (Experimental Physics and Industrial Control System) [4] [5].

A. RF Control System

Fig.3 shows the setup used for field test of the new RF control system. The rack contains a personal computer (PC) and the octal resonator controller (OCR). A block diagram is represented in Fig.2.

1) PC: The PC is equipped with a Linux operating system. The EPICS based I/O controller (IOC) allows input/output operations to OCR via USB and provides access to hardware parameters via the Channel Access protocol (a network protocol) in form of process variables (PVs). The EPICS IOC acts as server setting and retrieving data to/from the hardware. On the client side, a Graphical User Interface (GUI), based on Control System Studio (CSS) [6] allows an operator to monitor cavity signals, forward and reflected power on cavities, digital parameters of the hardware, switch on/off cavities, enable feedback loops, choose field and phase setpoints and other parameters, see Fig.4.

2) OCR: OCR essentially contains a RF I/O controller card (RF IOC), a RF front end board (RFFE), a Power Monitor board (PM), two DRS evaluation boards [7], an USB hub and eight Helical Resonator filters. The RF IOC will be detailed in the next section. The RFFE board is used to adapt the amplitude level of the RF signals from the pick-up port of the cavity to the ADCs of the RF IOC and from the DACs of the RF IOC to the power amplifiers and hence to the cavities.

Fig. 3. Rack. On the top there is the PC and under it there is the OCR

Fig. 4. CSS Interface for monitoring the working status of a cryostat. In the top corners the level of liquid Helium in the cryostat, on the left, and the pressure of the Helium, on the right, are monitored. For each cavity there is the possibility to read the forward power, the reflected power, the power in cavity, the gradient of the electric field and its phase in cavity.

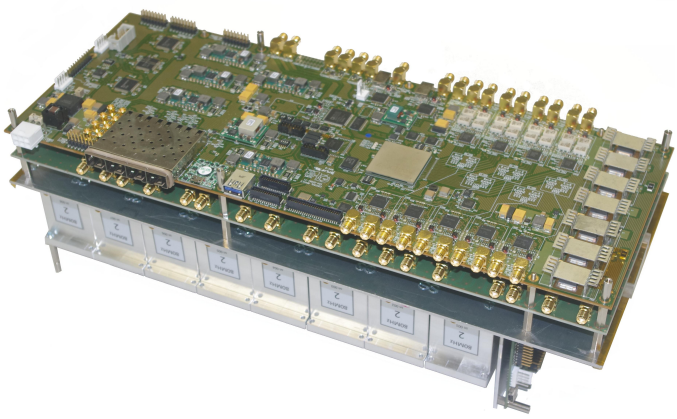
The PM board measures the reflected powers and the forward powers of the eight controlled cavities.
The Helical Resonator filters were designed, manufactured, tuned and tested at LNL. They exhibit a bandwidth of 1 MHz, 9 dB loss in centre band, a Q factor of 73 and -14 dB of return loss for the 80 MHz version, and a bandwidth of 3.6 MHz, 7 dB loss in centre band, a Q factor of 44 and -17 dB of return loss for the 160 MHz version.

B. RF IOC

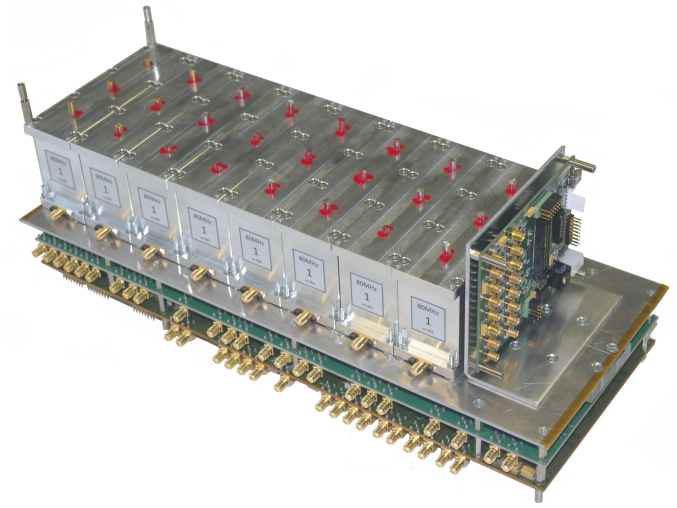
A digital RF controller (Fig.5a), based on direct RF sampling, has been designed and developed for this target. Each RF controller controls at the same time eight cavities. It is composed of RF ADCs for the direct sampling of the signals attenuated/amplified picked up from cavities, a Xilinx Kintek 7 FPGA for signal processing and RF DACs for driving power amplifiers and hence the cavities. The FPGA design mimics the control loop of the existing analog RF controller [3].

The controller can excite the cavities in two different modes of operation: the generator driven mode (GDR) and the Self Excited Loop mode (SEL). In the GDR mode the RF field is fed into the cavity by a frequency generator and there is the possibility to choose the desired magnitude and phase field in cavity. In SEL mode the controller, the power amplifier and the cavity resonator form a closed loop that, under adequate conditions, oscillates at a frequency determined essentially by the cavity parameters.

Fig.6 shows the block diagram of the firmware, implemented in VHDL, of the FPGA. The signal from the pick up antenna is digitized by RF ADC with a suitable sampling frequency, chosen in the way described in the next section. The digitized signals, possibly decimated, are demodulated in phase and quadrature components. To accomplish this operation the CORDIC algorithm in rotation mode is applied: from the two rectangular coordinates (in-phase and quadrature components), the phase and the amplitude (polar coordinates) of the RF field are obtained. Since phase and cavity field are meaningful physical properties, it is convenient to control



(a)



(b)

Fig. 5. Block containing the RF I/O controller board (RF IOC), the RF front end board (RFFFE), eight helical resonator filters and the power monitor board (PM). (a) Top view: on first plane there if the RF IOC and under it the RFFE. (b) Bottom view: in first plane there are the eight filters and on the right the PM.

them independently. The use of polar coordinates, allows their management with different control loops with independent proportional and integral gains.

The magnitude modulation is done by a proportional-integrative controller. On the magnitude correction is added a quiescent power whose value represents the power in the cavity when the feedback loops are open and in critical coupling condition.
The phase feedback loop depends on which operating mode of the cavity has been selected. In SEL mode the cavity phase signal is the sum of cavity phase and the phase shift imposed by the controller, while in GDR mode the phase signal represents the phase modulated by the PI block of the controller. In SEL mode a phase shift changes the length of the loops and consequently the resonantly frequency. Optimizing this value brings the auto-oscillating frequency close to the resonance frequency of the cavity and maximizes the auto-oscillating magnitude. Also in the phase feedback circuit the gain is set as high as possible, but avoiding auto-oscillation

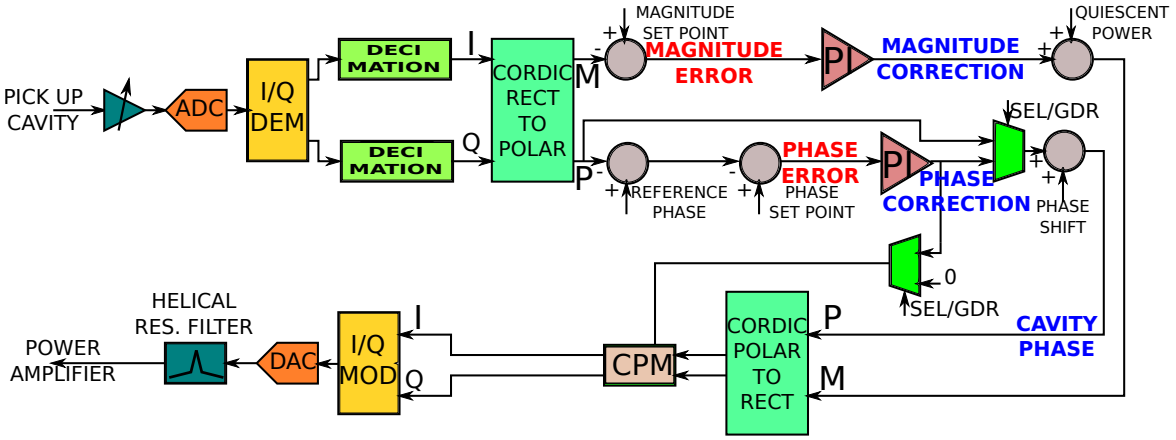


Fig. 6. FPGA Data flow.

of the circuit itself. The cavity phase and the magnitude so obtained are reconverted in rectangular coordinates using the CORDIC algorithm in vectoring mode. These coordinates are the inputs of the CPM block, which works by adding the in-phase and quadrature components of the correction signal. The phase correction signal is obtained by a comparison with the reference phase, too. With this signal it is possible to set the phase required to optimize the transit time factor of the particles in cavities. The in-phase and quadrature signals at the output of the CPM block are modulated, fed into the digital analogue converter, filtered with a narrow pass-band filter and routed to the power amplifier.

III. Analog-Digital conversion

The RF I/O controller board hosts four ADS42JB69, 16 bit, 250 MSPS analogue-to-digital converters. The maximum Nyquist frequency available with these ADCs is smaller than the RF frequencies of interest, so under-sampling is adopted. With this technique, the hardware complexity and the cost of the RF controller (RF IOC) is reduced since RF mixers and oscillators are no longer needed. The RF signal feeds an ADC at a sampling rate of $f_s = 1/T_s$. In order to extract the I/Q information [8] from these samples, the sampling frequency f_s for a correct down-conversion, has to be chosen following the relations:

$$f_{RF} = kf_s \pm \frac{f_s}{4}, \forall k \in Z | k \geq 1$$
$$f_s \geq 4B \qquad (1)$$

where f_{RF} is the resonance frequency of the cavities and B the bandwidth of the RF signal. These conditions ensure that a non-overlapped alias will appear centred at $f_s/4$.

The second relation of (1) indicates that the sampling frequency is related to the bandwidth of the signal. In our study, this condition is always met, because low and medium beta cavities have a bandwidth of Δf_{80} =0.26 Hz and Δf_{160} =2.61 Hz, respectively, Table IV.

The clock for the FPGA, ADCs and DACs is provided by two Dual/Cascade PLL LMK04828B. The first stage of the PLL is driven by a 160 MHz reference signal provided by the master oscillator at ALPI. An external CVHD-950 VCXO at 100 MHz provides the reference clock for the second stage of the PLL. The internal VCO of the second stage works in the range from 2415 MHz to 2460 MHz. To provide the right sampling frequency for the ADCs and meet the VCO range condition a factor D has to be inserted in (1), that can be rewritten as:

$$f_{RF} = \frac{1}{D}\left(kf_s \pm \frac{f_s}{4}\right), \forall k \in Z | k \geq 1 \qquad (2)$$

With signals sampled outside the first Nyquist zone, clock and aperture jitter have large impact on the resulting error. To reduce the impact a moving average of subsequent samples is implemented in FPGA.

IV. Performance test

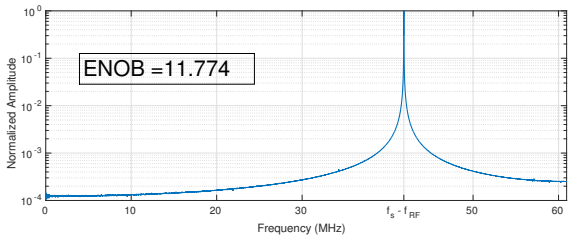
In this section both offline and field test measurements are reported. The offline measurements were made in laboratory test bench. The clock reference and the input test signals were generated using a R&S®SMW200A Vector Signal Generator. The field test measurements were taken directly in superconducting cavities, four low beta cavities and four medium beta cavities. Following equation 2, the sampling frequencies f_s has been chosen to yield the smallest k and to be equal both for f_{RF} = 80 MHz than for f_{RF} = 160 MHz. Table I lists the parameters that satisfy these requirements.

TABLE I
Values of equation 2

f_{RF} [MHz]	k	D	sign
80	5	8	+
160	5	4	+

A. ADC performances

During the offline tests the ENOB [10] of the ADCs were measured. The clock signal of the ADCs has a frequency $f_s = D \cdot 4f_{RF}/(4 \cdot k + 1) = 121.9$ MHz. A measure of the jitter is shown in Fig.8.
The upper limit of the ENOB was obtained shorting the



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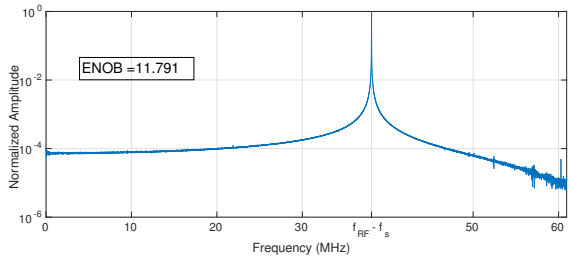


(b)

Fig. 7. Theoretical ENOB. (a) The simulated sinusoid has a frequency $f_{RF} = 80\,\text{MHz}$, (b) The simulated sinusoid has a frequency $f_{RF} = 160\,\text{MHz}$.

input of the ADC on a matched load, thus sampling the noise floor. A sinusoid computed via Matlab® was generated and overlapped to a normally distributed random sequence to simulate the quantization noise, in such a way that signal-to-noise ratio equals to $SNR = 6.02N + 1.76$. Adding the sampled noise floor and using the equation :

$$ENOB = \frac{SINAD - 1.76 + 20log(\frac{V_{fullscale}}{V_{input}})}{6.02} \quad (3)$$

the theoretical ENOB was found. In particular if the sinusoid has a frequency of 80 MHz, Fig.7a, ENOB= 11.77, while for frequency of 160 MHz, Fig.7b, ENOB= 11.79, Table II. These values are very close to the ENOB = 12 reported in data sheet of the ADCs used.

TABLE II
IDEAL ENOB

f_{RF} [MHz]	ENOB
80	11.77
160	11.79

TABLE III
REAL ENOB

f_{RF} [MHz]	ENOB
80	10.26
160	10.11

A signal with frequency of 80 MHz is applied at the input of the ADCs. To clean the test input signal from undesired harmonics a narrow bandpass filter centred at 80 MHz was interposed. The FFT magnitude of the sampled input signal at 80 MHz is show in Fig.9a and the ENOB, calculated following the equation (3), is $\text{ENOB}_{80} = 10.26$. The same test was repeated to reveal that at 160 MHz $\text{ENOB}_{160} = 10.11$, Fig.9b, Table III.

In RF sampling ADC, the noise is dominated by the external clock jitter. The limitation to SNR [11] based only on clock jitter can be determined by the equation :

$$SNR = -20log(2\pi f t_j) \quad (4)$$

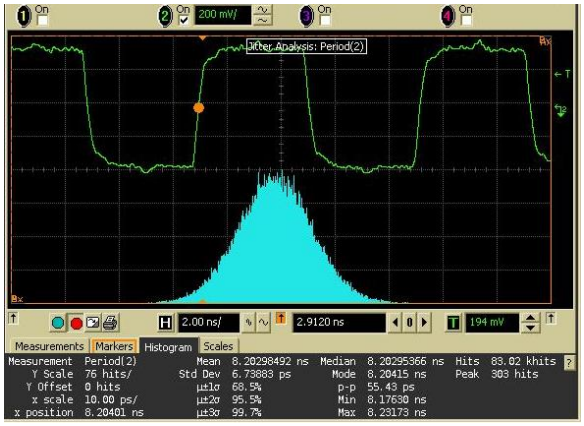
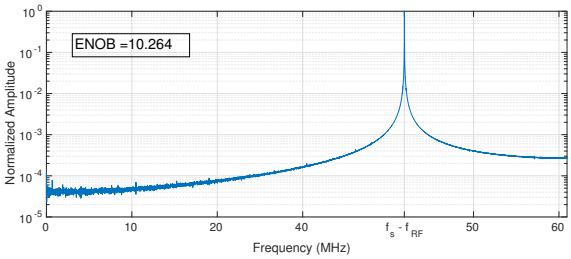
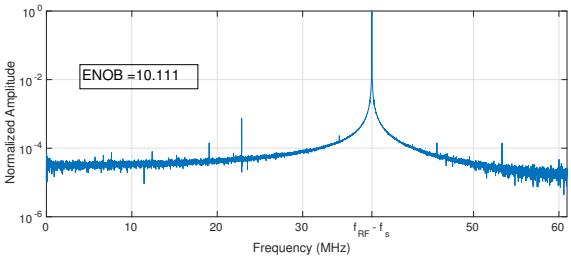


Fig. 8. Clock signal of the ADCs.



(a)



(b)

Fig. 9. Measured ENOB. (a) The sinusoidal input test signal has a frequency $f_{RF} = 80\,\text{MHz}$, (b) The sinusoidal input test signal has a frequency $f_{RF} = 160\,\text{MHz}$.

where t_j is the time jitter. As mentioned before, to reduce the effect of the frequency noise and so increase the signal to noise ratio, a moving average between samples can be done.

B. New RF control system performances

We first evaluated the drift of the phase signal at the output of the first CORDIC block versus the temperature. As shown in Fig.11a and in Fig.11b a value of $-0.22°/°\text{C}$ was found.

As written above the performance of the new RF control system has been tested with four cavities at 80 MHz and four cavities at 160 MHz in superconducting conditions. The low beta cavities (80 MHz) have a loaded quality factor $Q_L = 3.13 \times 10^8$. The medium beta cavities (160 MHz) have a loaded quality factor $Q_L = 6.13 \times 10^7$, Table IV. The values of Q_L were measured [9] using the decay method in critical coupling condition. The phase and magnitude stability were evaluated with an accelerated beam current of few nA of ^{32}S and eight phase and amplitude locked cavities. In

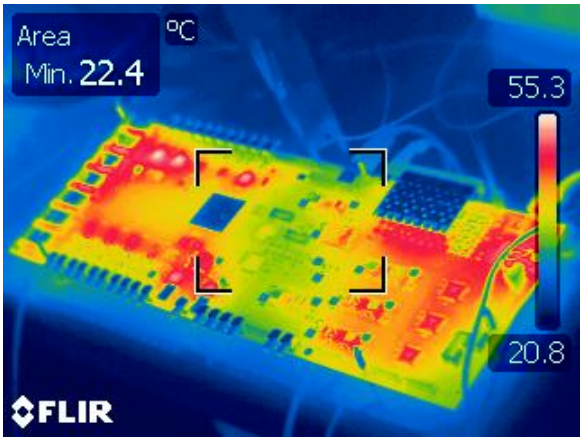
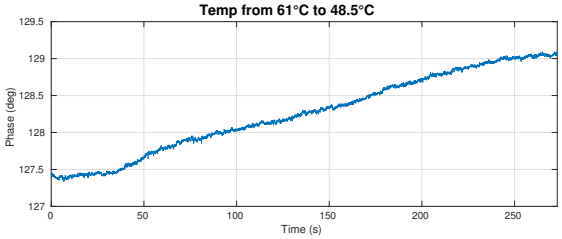
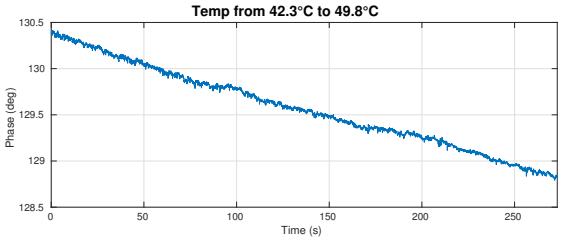


Fig. 10. Thermal photo of the RF I/O controller board.



(a)

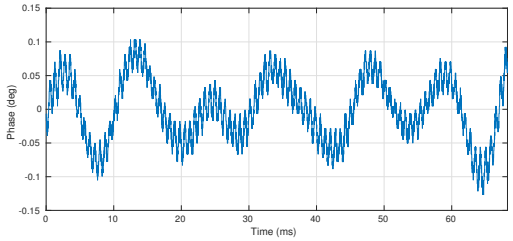


(b)

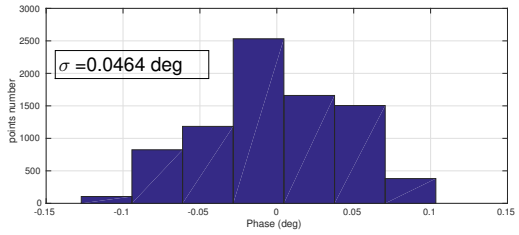
Fig. 11. Phase drift in time when the temperature measured in the RF IOC changes from 61 °C to 48.5 °C in (a) and from 42.3 °C to 49.8 °C in (b).

the course of the testing sessions, the magnitude and phase loops were locked in SEL mode. Fig.12 and Fig.13 show the phase and magnitude error during SEL operation for a low beta cavity. The phase error is $0.046°$ rms and the total relative magnitude error is $2.16 \cdot 10^{-4}$ rms. Fig.14 and Fig.15 show the phase and magnitude error during SEL operation for a medium beta cavity. The phase error is $0.011°$ rms and the total relative magnitude error is $1.54 \cdot 10^{-4}$ rms. The difference in the performance of low and medium beta cavities depends essentially on the physics of the cavities. Low beta cavities are more sensitive to microphonics perturbations (e.g. a pressure variation of the helium bath cause a resonance frequency movement of $1\,\mathrm{Hz/mbar}$ for low beta cavities and of $0.01\,\mathrm{Hz/mbar}$ for medium beta cavities).

We also tested the robustness of the feedback control loop, in phase and in amplitude. This was done studying the transient response [12] of the RF field in the cavity changing the setpoints in amplitude and phase. The cavity transient response, as general rule, needs to be as fast as possible without overshoots or ringing. The transient responses are

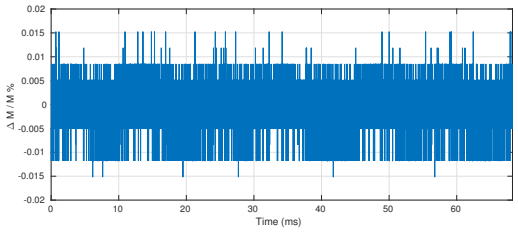


(a)

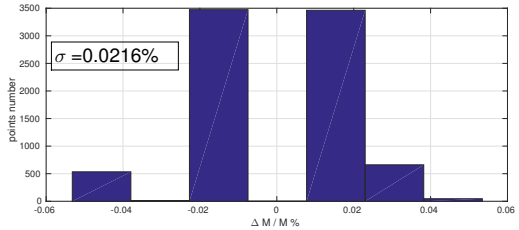


(b)

Fig. 12. Phase error (a) and distribution of its value (b) for a low beta cavity running in SEL mode.



(a)



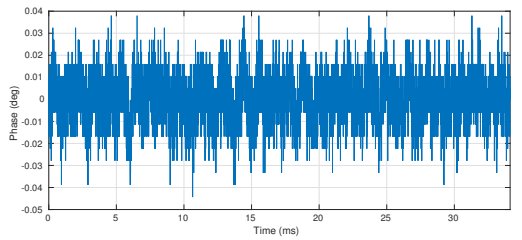
(b)

Fig. 13. Field magnitude error (a) and distribution of its value (b) for a low beta cavity running in SEL mode.

shown in Fig. 16 for a low beta cavity and in Fig.17 for a medium beta cavity. In order to fulfil these requirements the delay of the electronics and the latency of the FPGA firmware should be as low as possible. The time constant τ governing the cavities is $\tau = 0.623\,\mathrm{s}$ for low beta cavities, while for medium beta cavities $\tau = 0.061\,\mathrm{s}$, Table IV. The gains of the PI controllers have to be tuned so that the time constant of the feedback loop approaches the time constant τ of the cavity.

TABLE IV
CAVITY CHARACTERISTICS

Cavity Type	f [MHz]	τ [s]	$Q_L = \omega \cdot \tau$	$\Delta f = f/Q_L$ [Hz]
Low Beta	80	0.623	$3.13 \cdot 10^8$	0.26
Medium Beta	160	0.061	$6.13 \cdot 10^7$	2.61



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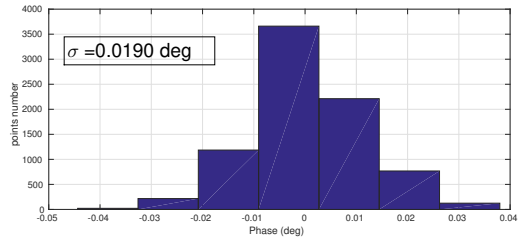
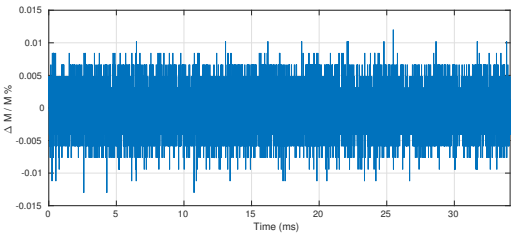
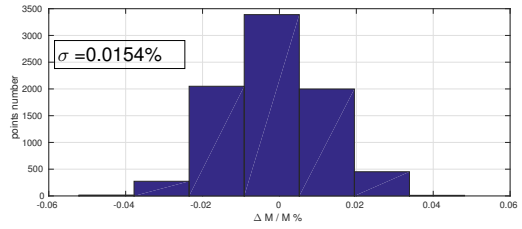


(b)

Fig. 14. Phase error (a) and distribution of its value (b) for a medium beta cavity running in SEL mode.



(a)



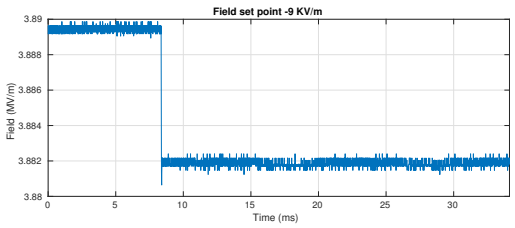
(b)

Fig. 15. Field magnitude error (a) and distribution of its value (b) for a medium beta cavity running in SEL mode.

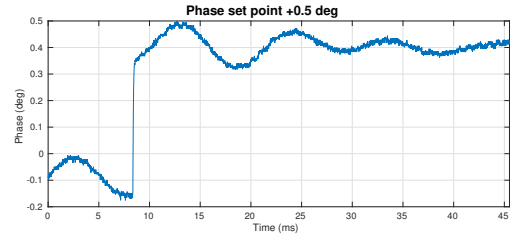
V. Conclusions and Outlook

This RF controller has been used to keep phase and amplitude locked eight cavities for a few days. In this time the controller has proven to be as stable and reliable as the old analogue system and to respect phase and amplitude field stability requirements. A temperature dependency has come into evidence with the Low-Level Radio Frequency (LLRF) system. To reduce this problem two solutions are under investigation: one possible solution is to regulate the speed of the cooling fans in the box controller depending on the measured air temperature, the second is to place the controller in a cooled temperature-stabilized rack.

An excessive clock jitter of $55.4\,\mathrm{ps}$ p-p has been measured in the controller board. The noise reduces the signal to noise ratio and the signal to noise and distortion ratio. To increase the ENOB it is advisable to reduce the jitter with a careful clock distribution network on the printed circuit board.

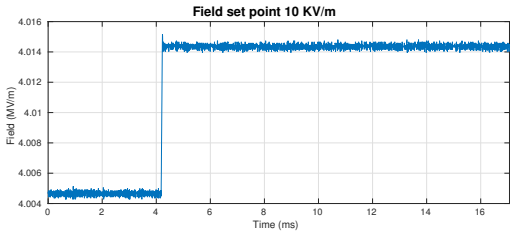


(a)

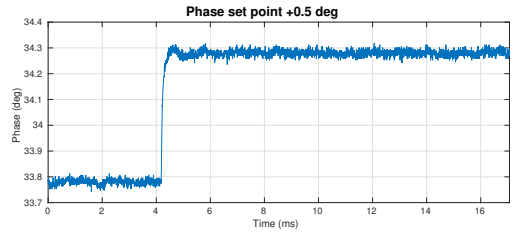


(b)

Fig. 16. Step response of the field magnitude (a) and of the phase (b) for a low beta cavity.



(a)



(b)

Fig. 17. Step response of the field magnitude (a) and of the phase (b) for a medium beta cavity.

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