High Speed Continuous DAQ System for Readout of the ALICE SAMPA ASIC

Ganesh Tambave and Arild Velure for the ALICE collaboration

Abstract—During the Long Shutdown 2 of CERN's LHC, foreseen to start in 2018, the ALICE experiment will upgrade its TPC detector to cope with the higher Pb-Pb collision-rate in the next running phase. In the upgraded TPC, Gas Electron Multiplier technology and continuous readout will replace the existing Multi-Wire Proportional chambers and triggered readout system. The Gas Electron Multiplier signals will be processed using a new custom mixed-signal front-end chip named SAMPA. The first version of SAMPA was delivered in 2014 and the production of the final version is in progress. This article gives an overview of the data acquisition system design used for testing the first version of SAMPA and its performance results with SAMPA coupled to a GEM detector prototype.

I. INTRODUCTION

Por Run 3 and onward of the ALICE experiment, the Pb-Pb collision rate of the CERN's Large Hadron Collider (LHC) is expected to reach a rate up to 50 times higher than the present rate with considerable increase in the integrated luminosity (from 1 nb⁻¹ to 10 nb⁻¹) [1]. To make full use of the increased luminosity the current Multi-Wire Proportional chambers of the ALICE Time Projection Chamber (TPC) will be replaced by readout chambers featuring Gas Electron Multiplier (GEM) foils [2]. Since the new interaction intervals will be shorter than the particle drift time in the detector, a triggerless, continuous readout will replace the existing triggered readout.

The signals arriving from the GEMs will be processed by front-end cards each consisting of five custom-made SAMPA ASICs and two GigaBit Transceivers (GBTx). Each SAMPA ASIC will have 32 individual signal processing channels. The data from these channels will further be multiplexed and transmitted using GBTx via optical links to a Common Readout Unit (CRU). The CRU is an interface to the on-line computer farm, trigger and detector control system.

The first prototype of the SAMPA ASIC with three channels was recently produced. To test its performance, a continuous data acquisition system was developed using an Altera System-on-Chip development board with Cyclone-V FPGA. A custom board was designed for the SAMPA to mount directly on the FPGA board. Data packets from the SAMPA are read out over a GigaBit Ethernet link provided by this board. The data samples are then stored in ROOT files as well as being analysed in real-time using the CERN ROOT data analysis

Manuscript received May 30, 2016.

Both authors are with the Department of Physics and Technology, University of Bergen, P.O. Box 7800, NO-5020 Bergen, Norway (e-mail: Ganesh.Tambaye@uib.no and Arild.Velure@uib.no).

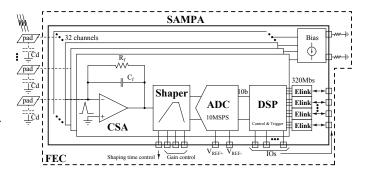


Fig. 1. Block diagram of the SAMPA ASIC consisting of Charge-Sensitive preAmplifier (CSA), Shaper, Analog-to-Digital Converter (ADC) and Digital Signal Processing (DSP) block made up of different data filters.

framework to monitor the data quality. To control, configure, and monitor the SAMPA and the FPGA board, a software-package with a graphical user interface was developed. The data acquisition system was successfully used for testing the three channel readout and is also easily scalable to 32 channels using data compression capabilities of the SAMPA chip. In the following sections the readout-system design and its performance tests of the SAMPA is discussed.

II. SAMPA ASIC

The SAMPA ASIC is designed for the upgraded front-end electronics of the ALICE TPC as well as the ALICE Muon Chambers. The SAMPA ASIC is a 32 readout channel device containing a charge-sensitive pre-amplifier (CSA), a pulse shaper, an ADC and a corresponding DSP chain as shown in Fig. 1.

The charge-sensitive pre-amplifier integrates the input charge using the feedback capacitor (C_f) . A parallel largeohmic resistor (R_f) resets the amplifier after each pulse. The following pulse shaping element creates a 4^{th} order semi-Gaussian shape of the output voltage from the charge-sensitive pre-amplifier. Followingly, the signal from the shaper is digitized using a successive approximation type ADC with 10 bit resolution and 10 MHz sampling rate. The Digital Signal Processing (DSP) section provides different filters like baselineline correction, tail cancellation, zero-suppression and data compression. More details on the ALICE TPC requirements for the SAMPA can be found in [3] [4]. The first prototype of the SAMPA is made in a 130 nm CMOS technology. The fabricated front-end is designed with selectable peaking times of 80 ns, 160 ns and 300 ns, selectable gains of 4 mV/fC, 20 mV/fC and 30 mV/fC. The outputs have an Equivalent

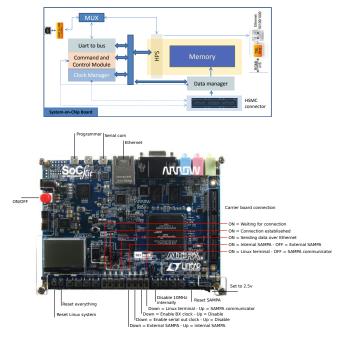


Fig. 2. Top: Schematic overview of the firmware design showing various system blocks. Bottom: Photograph of Altera SocKit board containing an Altera Cyclone V System-on-Chip FPGA. Different functional points of the board are denoted using arrow.

Noise Charge (ENC) of 428 e, 10 bit resolution, and 20 MHz sampling frequency.

III. HIGH SPEED DATA ACQUISITION SYSTEM

The FPGA based data acquisition system is specially designed for acquiring data, doing verifications and automatic self-tests on a SAMPA front end chip. It is designed around an Altera SocKit evaluation board containing an Altera Cyclone V System-on-Chip FPGA, which has a built in dual core ARM Cortex-A9 microprocessor unit. A block diagram of the firmware design and a photograph of the Altera SocKit board is shown in Fig. 2. The SAMPA chip has 11 differential data links running at 320 Mbps adding up to 3.52 Gbps. Data from these links are aggregated and stored in memory shared with the microprocessor. A program running on the Linux system of the System-on-Chip compresses the data on the fly and transmits it over Ethernet to the controlling computer.

On the computer, a ROOT program is running which receives the data, displays it and is able to run analysis in real time. A graphical user interface has been developed to simplify run control for the user. Easy access to control settings, e.g. to change sampling speed, data flow-control, which stimuli to inject etc. and to display status information for both the SAMPA and the DAQ is provided. The system was successfully used for testing the first SAMPA prototype and will also be used in testing of the second prototype arriving this summer. The test performance of the DAQ system is discussed in the following section.

IV. TEST SETUP, RESULTS AND DISCUSSION

The high-speed DAQ system performance tests were carried out using pulse generator or GEM detector prototype as signal

sources, depicted in Fig. 3.

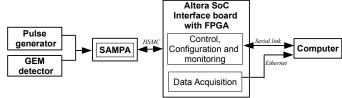


Fig. 3. Schematic overview of the experimental setup. Pulse generator or GEM detector signals are injected into the SAMPA and read out using the FPGA board.

To perform feature extractions (amplitude, time etc.) from the recorded signals, different methods such as peak search, area of waveform and waveform fitting are used. A semi-Gaussian function of the fourth order is used for fitting the waveform [5].

A. Signal injection using pulse generator

The test charge was injected into the SAMPA chip by sending a ramp signal through 1 pF series capacitor. The frequency of ramp signal was $10\,\mathrm{kHz}$, symmetry was set to $100\,\%$ and output impedance was $50\,\Omega$. During the experiment, the device under test was kept inside a Faraday cage to shield it from external noise sources.

Different signal extraction methods have been tried out, in order to verify their performances with respect to complexity and accuracy. For this, a fixed amplitude test waveform was injected into the SAMPA chip. The pulse height distributions obtained using three different methods are shown in Fig. 4. Since it can be concluded that the waveform fitting is the best suited method, it was also used for the test carried out using the GEM detector. The reason for poor the performance of the peak search method is a combination of relatively low sampling rate of the ADC (10 MHz) and the selected short shaping time of 160 ns, which gives an average waveform length of only three samples.

The SAMPA chip can be operated with different gains as well as at different peaking times, requiring many tests to cover all combinations. As an example, the gain linearity has been verified by plotting the relation between the waveform amplitude and integral (sum of samples in the signal region) of the waveform as shown in left plots of Fig. 5. Here, the size of the blobs corresponds to the number of waveforms used to study the particular input charge value. The input charge was varied from 2 fC to 26 fC acquiring 1000 waveforms for each setting.

It is assumed that if the waveform shape is stable for different input charges then the ratio of waveform integral (I) over amplitude (A) must be constant. Therefore, to verify the waveform stability, the ratio of I over A is plotted against A as shown in the right plot of Fig. 5. The constant trend of the I over A ratio confirms that the waveform shapes are stable for various input charges.

The peaking time stability over various waveform amplitudes or input charges was verified by plotting the waveform amplitude as function of peaking time shown in Fig. 6 (Left)

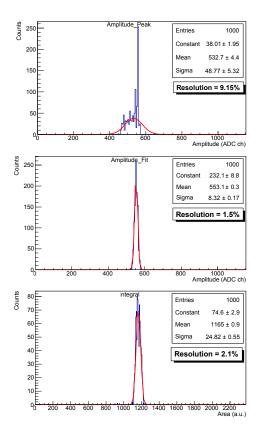


Fig. 4. Pulse height distribution obtained using Peak search (top), Fit to the waveform (middle), Integrating samples in the signal region (bottom). The input charge value is 25 fC for the SAMPA gain 20 mV/fC.

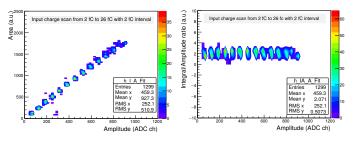


Fig. 5. Left: Waveform integral versus the waveform amplitude. Right: Ratio of integral over amplitude versus amplitude. The gain setting was 30 mV/fC. The waveform amplitude and integral of samples varies linearly with input charge and the constant nature of the integral over amplitude ratio confirms the waveform shape stability.

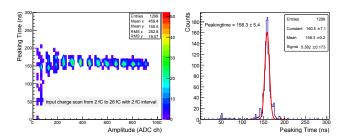


Fig. 6. Left: A peaking time of the waveform versus the waveform amplitude. Right: A y-projection of left plot. The gain setting was 30 mV/fC. The peaking time is almost constant for various waveform amplitudes or input charges.

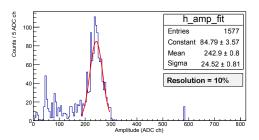


Fig. 7. Fe-55 soft-photon energy spectrum obtained using waveform fitting method. The energy resolution for $5.9\,\mathrm{keV}$ photons is $10\,\%$.

and its y-projection is shown in Fig. 6 (Right). The peaking time was set to $160 \, \text{ns}$ for this test and the measured value $158.3 \pm 5.4 \, \text{ns}$ is close to the set value.

B. Using GEM detector prototype

The upgraded ALICE TPC will make use of GEM foil readout chambers. Hence, to have a realistic test environment, the DAQ system has been tested with a prototype GEM detector. The detector consists of stack of three standard sized GEM foils. To initiate the processes of excitation and ionization inside the GEM detector, a Fe-55 radioactive source was used. The photons emitted by the Fe-55 (5.9 keV) interact with the detector gas as maximum ionizing particles through the photoelectric effect.

The Fe-55 soft-photon energy spectrum was obtained using a fit to the signals as shown in Fig. 7, taken for a detector readout pad size of $6\,\mathrm{mm}\times15\,\mathrm{mm}$ with $\mathrm{NeCO_2N_2}$ gas mixture. For this spectrum, the gain of the GEM detector was 2000 and the gain of the SAMPA chip was 20 mV/fC. The measured energy resolution is 10 % and is in agreement with the requirements for the ALICE TPC.

V. OUTLOOK AND CONCLUSION

To test the SAMPA ASIC developed as a part of ALICE TPC upgrade, a high-speed data acquisition has been designed and successfully tested using signal generator as well as a GEM detector. General tests such as gain linearity, pulse shape and peaking time stability were carried out for various values of the SAMPA input charge. A good gain linearity and pulse shape stability has been observed. The design requirements and measured peaking time values are in good agreement. Also, the DAQ system has performed very well while it was coupled to the GEM detector. Energy resolution of 10% is obtained for Fe-55 soft photons of 5.9 keV energy in NeCO₂N₂ gas mixture at a GEM detector gain of 2000. The production of the second prototype of the SAMPA ASIC with 32 readout channels is in progress and it will be delivered in July 2016. The DAQ system reported in this paper with some updates will also be used to test the performance of the second prototype.

ACKNOWLEDGMENT

We would like to thank ALICE TPC collaboration, the SAMPA ASIC design team, and Dezso Varga from Wigner research institute, Budapest, Hungary for providing the GEM chamber.

REFERENCES

- The ALICE Collaboration, "The ALICE Experiment at the CERN LHC," *Journal of Instrumentation*, vol. 3, no. 08, p. S08002, 2008.
 The ALICE Collaboration, "Upgrade of the ALICE Time Projection Chamber," Technical Design Report, CERN-LHCC-2013-020, ALICE-TED 016, 2012. TDR-016, 2013.
- [3] A. Velure, "Upgrades of the ALICE TPC front-end electronics for Long Shutdown 1 and 2," *IEEE Transactions on Nuclear Science*, vol. 62, no. 3, pp. 1040-1044, June 2015.
- [4] H. Hernandez, W. V. Noije, and M. Munhoz, "Configurable low noise readout front-end for gaseous detectors in 130 nm CMOS technology," in 2015 IEEE International Symposium on Circuits and Systems (ISCAS), May 2015, pp. 1058–1061. [5] R. Bramm, "Characterisation of the ALICE TPC readout chip," Ph.D.
- dissertation, Goethe-Universität Frankfurt am Main, Frankfurt, Germany,