Development of ATLAS Liquid Argon Calorimeters Readout Electronics for HL-LHC

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***Abstract*—The high-luminosity phase of the Large Hadron Collider (LHC) will provide 5-7 times greater instantaneous and total luminosities than assumed in the original design of the ATLAS Liquid Argon (LAr) Calorimeters and their readout system. The improved trigger system has a higher acceptance rate of 1 MHz and a longer latency of up to 60 micro-seconds. This requires an upgrade of the readout electronics, and a better radiation tolerance is also required. This paper will present concepts for the future readout of the 182,468 calorimeter channels at 40 or 80 MHz with a 16 bit dynamic range. Progress of the development of low-noise, low-power and high-bandwidth electronic components will be presented. These include radiation-tolerant preamplifiers, analog-to-digital converters (ADC) up to 14 bits and low-power optical links providing transfer rates of at least 10 Gbps per fiber.**

***Index Terms*—ATLAS, Liquid Argon Calorimeters, Readout Electronics.**

I. Introduction

As the LHC run plan shown in Figure 1, the LHC will be upgraded to HL-LHC (High Luminosity LHC) after Run 3. HL-LHC will have an instantaneous luminosity of 5-7$\times 10^{34}$ cm^{-2}s^{-1}, with the ability to provide an integrated luminosity of 3-4.2 ab^{-1} after 12 years of running. The LAr calorimeters are used in the electromagnetic barrel, electromagnetic endcap, hadronic endcap and forward calorimeters of the ATLAS detector [1]. There is a total of 182,468 calorimeter cells [2]. We will focus here on the upgrades that are planned for Phase-2, after the phase-1 upgrades will have be completed.

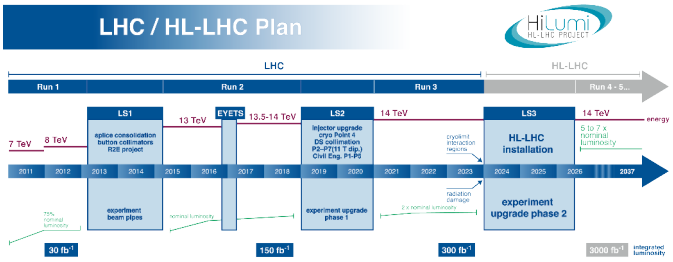

Fig. 1: Run plan of LHC and HL-LHC [3]

Figure 2 shows the readout architecture of Phase-I upgrade [5]. The signals with higher spatial granularity are digitized and processed. After the third long shutdown, main readout electronics of the ATLAS LAr calorimeters will be upgraded for Phase-II as shown in Figure 3. Readout of all calorimeter cells will be sampled by the ADC with 14 bit resolution to cover the 16 bit calorimeter signal, without trigger selection. To mitigate the pile-up effects in energy reconstruction, the second trigger level can get calibrated energies of all cells at a rate of 1 MHz. For the new architecture, the hardware based first level trigger will be divided into two levels (Level-0 and Level-1). The main function of Level-0 trigger is done by LAr Trigger Digitizer Board (LTDB), LAr Digital Processing System (LDPS), and the Feature Extractor (FEX) systems installed in Phase-I upgrade. The Level-1 trigger will access the full granularity detector information to further enhance discrimination against backgrounds [4].

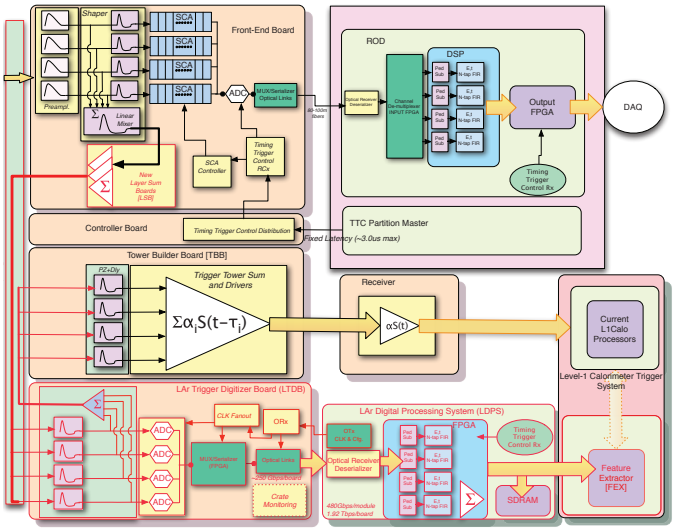

Fig. 2: Schematic block diagram of the LAr Phase-I upgrade trigger readout architecture. The new components are indicated by the red outlines and arrows. [5]

In the front-end, the legacy trigger electronics (mainly the tower builder board) will be decommissioned. The LTDB and LDPS installed in Phase-I upgrade will be kept for the Level-0 trigger. Main readout electronics with new Front-End Boards (FEB2) will amplify and shape the calorimeter cell signals, and digitize them with ADC running at 40 MHz or 80 MHz sampling frequency. The digitized data will be directly sent over high-speed optical links to the new back-end board LAr Pre-Processor Boards (LPPR). In total there will be 60-120 LPPRs in Advanced Telecommunications Computing Architecture (ATCA) crates. The LPPR will use the Phase-I LAr Digital Processing Blades (LDPB) board as the prototype. High performance signal filtering methods will be implemented in the FPGAs [6]. The amplitude and timing of a signal pulse can be obtained.

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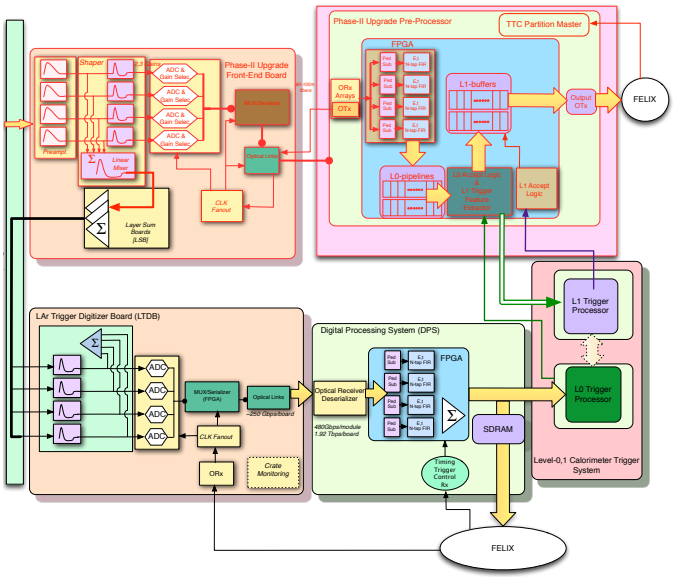

Fig. 3: The readout architecture for LAr Phase II upgrade [7]

II. ASIC Research and Development

The front-end electronics need to be radiation tolerant and low power consumption. The radiation tolerance requirement for the FEB2 will be about 300 kRad. Compared to the old FEB, most of the functions will be implemented by ASICs on the new one, like the pre-amplifier, shaper, ADC and the serializer. Some research and development is ongoing with 65 nm and 130 nm CMOS technologies.

For the front-end analog part, the termination and dynamic range are programmable, they can be 25 ohm with 10 mA range, or 50 ohm with 2 mA range. There will be a low gain output and a high gain output in both cases. Two parallel investigations are on the way. One design employs the 65 nm CMOS technology for a fully-differential preamplifier (shown in Figure 4) and a shaper using 1.2 V power [8]. Capacitive feedback is used to set the gain, and to decrease the noise. The simulation shows that the linearity is within 0.2% at 8 mA range, and within 0.4% for 9 mA range. The noise is 160 nA for a 1.3 nF detector capacitance.

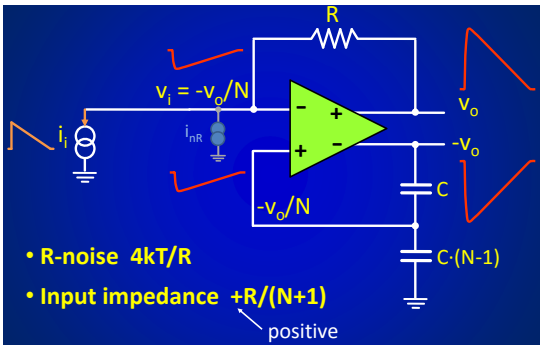

Fig. 4: The fully differential preamplifier in 65 nm CMOS technology [8]

Another design containing a preamplifier is with 130 nm CMOS technology [8]. The power supply is 2.5 V. The simulation shows that the noise is 150 nA with 1.5 nF detector capacitance. The integral non-linearity with CR-RC^2 shaping is within 0.2%. The 8 channels prototype has been submitted in April 2016. Figure 5 shows the layout of this chip. A common test bench named Front-End Test Board (FETB) is being developed for both ASICs, aiming to obtain preliminary results in late 2016 and early 2017.

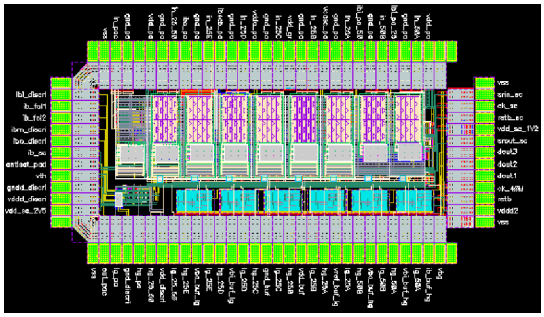

Fig. 5: Layout of the 8 channel preamplifier in 130 nm CMOS technology [8]

A radiation-tolerant redundant SAR (Successive Approximation) ADC prototype with 65 nm Global Foundry CMOS technology has been designed, as depicted in Figure 6. With the pipeline architecture, bit number in the first stage is chosen to be 9 bits, which allows fast conversion speed. A SEE detector is formed by a pair of resistors, a subtract current amplifier and some digital logic. Layout of the ADC is shown in Figure 7. When SEE occurs in one split-ADC, outputs of the two ADCs will be different. By analyzing the outputs, SEE detection circuits will discard the digital output from the ADC which is hit by the ionizing particle and choose the other output as the final output.

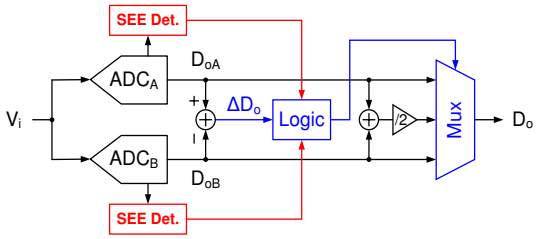

Fig. 6: Architecture of the SAR ADC in 65 nm CMOS technology [9]

The first ADC prototype has been tested, and large Digital-to-Analog Converter (DAC) mismatch is observed due to a layout error: some area is not filled with dummy around the SAR. Focused Ion Beam (FIB) surgery is performed to reduce the most significant bit capacitor size by cutting the metal-oxide-metal capacitor fingers. After the FIB, the preliminary result shows a 12.1 bits ENOB measured at 10 MHz input for a 40 Msps sampling rate [10].

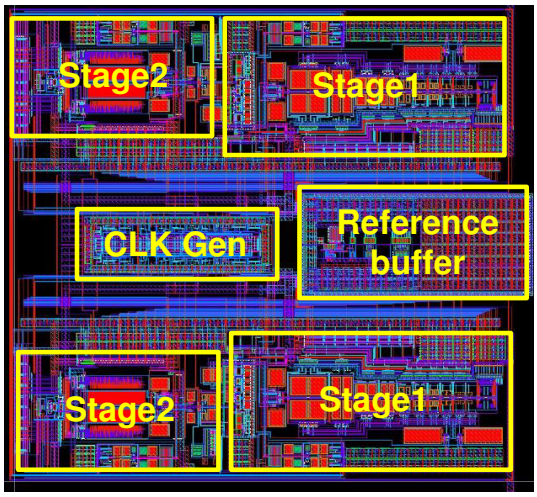

Fig. 7: Layout of the SAR ADC [9]

As part of the versatile link development [11], the VLAD (VCSEL Array Driver) and its low power version low power VLAD (lpVLAD) have being designed in the 65 nm CMOS technology. The aim is to include 8 to 12 VLAD lanes in an array optical transmitter (ATx). Figure 8 shows its

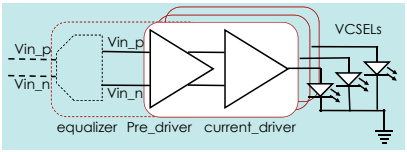

Fig. 8: Architecture of the VLAD

architecture. The two-stage pre-driver has a bandwidth of 12.5 GHz. Amplitude of its output is 700 mV, which is enough for the vertical cavity surface emitting laser. The post layout simulations indicate that the power consumption is 35 mW per channel for VLAD, and 20 mW per channel for lpVLAD. Both prototypes are in 65 nm TSMC process. Figure 9 shows their layout. The test is expected in summer of 2016.

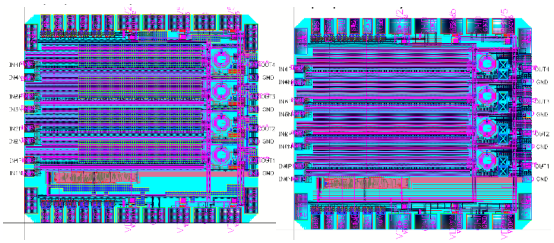

Fig. 9: Layout of the VLAD and lpVLAD

III. Conclusion

The new LAr calorimeter main readout system will be designed for the Phase-II upgrade. All of the FEBs will be replaced with a new design. The back-end electronics will also be upgraded to be compatible with the new two-stage hardware trigger. Research and development of ASICs is ongoing, and some preliminary results will be obtained. Depending on the results, the basic requirement will be to integrate the preamplifier and shaper. The desirable design will be to integrate the ADC. The best design is to also integrate serializer, and form an Front-End System On Chip (FESOC) for LAr readout for HL-LHC. The plan is to install the new readout electronics on the ATLAS detector during the third long shutdown in 2024 to 2026.

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