# Readout Electronics for the Belle II Imaging Time-Of-Propagation Detector

Dmitri Kotchetkov, *Member, IEEE,* Matthew Andrew, Thomas Browder, Julien Cercillieux, Steven Covin, Shawn Dubey, Christopher Ketter, Luca Macchiarulo, Curtis McLellan, Marc Rosen, Ziru Sang, Roy Tom, Gary Varner, *Member, IEEE*

Department of Physics and Astronomy, University of Hawaii at Manoa, HI 96822, U.S.A.

## Belle II Experiment

Flavor physics; search for new particles and processes beyond Standard Model predictions



iTOP

Collisions:
e+ (4 GeV)
e- (7 GeV)
$8 \times 10^{35}$ cm$^{-2}$s$^{-1}$

Particle identification:
99% of K/$\pi$ separation
for B -> $\rho\gamma$  (0.5% fake $\pi$ probability)

Barrel imaging Time-Of-Propagation detector (iTOP)

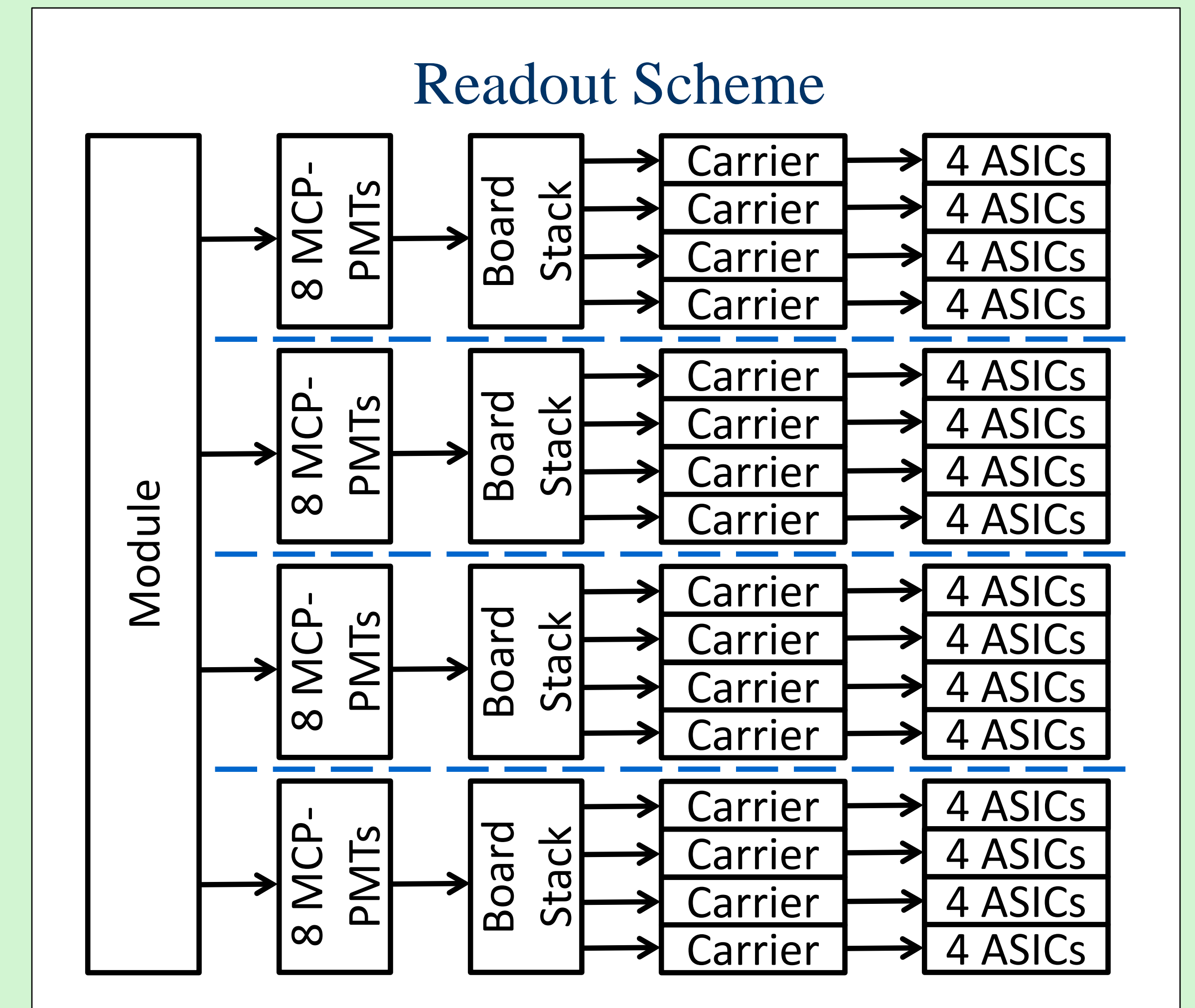## Cerenkov Particle Identification

iTOP = 16 staves



Cerenkov photon from a pion

quartz

charged particle

Cerenkov photon from a kaon

Cherenkov photons are detected by 2 x 16 array of 4 x 4 pixel microchannel plate photomultiplier tubes (MCP-PMTs)

3-D reconstruction: x- and y- coordinates and time

## Readout Scheme



Module → 8 MCP-PMTs → Board Stack → Carrier → 4 ASICs

## Switched Capacitor Storage Cell



Write Strobe
Trigger
Vin
T1
T2
to ADC
Csample
Vpedestal

16 x 32 windows (x 64 samples) Switched Capacitor Array for every channel

## Wilkinson ADC



Vin
Vramp
Vcomp
time

Comparator
Register
D (0:11)
Ramp Generator
Clock
Gray Code Counter
12

## ASIC

| | |
|---|---|
| Channels: | 8 |
| Storage cells/channel: | 32,768 |
| Timing strobe: | 1 |
| Analog bandwidth: | > 1GHz |
| Sampling rate: | 1-4 GSa/s  (adjustable) |
| Conversion cycle: | < 1µs  (for 512 windows) |
| Full chip readout: | ~ 10 ms |
| Event size: | ~ 1 MB (per ASIC) |
| Operation mode: | continuous storage/readout |

Four ASICs are mounted on one Carrier board
Total board stacks = 64

Total ASICs = 1024          Total channels = 8192

## ASIC Carrier



Pogo Pin Assemblies
Amplifiers
Connectors to ASIC Carrier
ASIC
Connectors to ASIC Carrier or SCROD
Zynq Z-7030

## SCROD
Standard Control Read-Out Data board



Debugging
Connectors to ASIC Carrier
Trigger Link
Data Link
Programming and Clock
Low Voltage Power
Zynq Z-7045

## Board Stack



1 SCROD + 4 Carriers
4 x 32 = 128 channels
128/16 = 8 MCP-PMTs
Anodized aluminum heat sinks

The board stack is attached to a high voltage resistive divider

ASIC Carrier pogo pins are pressed against Front Board pads connected to the MCP-PMT anode wires

## ASIC Carrier Standalone Performance



ASIC channel time resolution from 20 ns delay measurements is from 20 ps to 30 ps.

Emulator of MCP-PMT anode signal

## Board Stack Performance



Channel time resolution of the MCP-PMT signal when the pixels are illuminated by the laser single photons with pulse widths of ~30 ps is from 60 ps to 90 ps.

## COPPER

Common Pipelined Platform for Electronic Readout



High Speed Link Board (HSLB)
1.6 GHz Intel Atom CPU (32-bit)
Global Clock and Trigger

9U VME
Remote boot
Scientific Linux 5

One HSLB per one board stack
One COPPER board per one iTOP Module

Event size = 4 kB/channel (with 2.5% occupancy)