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Register-Like Block RAM: Implementation, Testing in FPGA and Applications for High Energy Physics Trigger Systems

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In high energy physics experiment trigger systems, block memories are utilized for various purposes, especially in indexed searching algorithms. It is often demanded to globally reset all memory locations between different events which is a feature not supported in regular block memories. Another common demand is to be able to update the contents in any memory location in a single clock cycle. These two demands can be fulfilled with registers but the cost of using registers for large memory is unaffordable. In this paper, a register-like block memory design scheme is presented, which allows updating memory locations in single clock cycle and effectively resetting entire memory within a single clock. The implementation and test results are also discussed.

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