Operational Experience with the Readout System of the MINOS Vertex Tracker

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***Abstract*–The MINOS vertex tracker is a compact instrument built for in-beam spectroscopy of exotic nuclei. Its main component is a ~30 cm long hollow cylinder shape time projection chamber (TPC) surrounding a liquid hydrogen target. The anode of the TPC is read out by a Micromegas detector segmented in 18 concentric rings of 2 mm × 2 mm pads totaling 3604 channels. A dedicated system based on the AFTER and AGET chips was designed to read out this TPC, and the required software to configure, monitor and acquire data was developed.**

After a construction period of two years and the validation of the instrument in a test beam, four nuclear physics experiments exploiting MINOS have been successfully conducted at RIKEN, Japan. We describe the prominent aspects of the readout system of MINOS and we report on lessons learned during the three years of exploitation.

I. Introduction

THE objective of the MINOS (MagIc Numbers Off Stability) collaboration is to study unstable exotic nuclei produced by proton induced knock-out reactions of a beam impinging a liquid hydrogen target [1]. MINOS uses a thick target to provide the increase of luminosity needed to accumulate sufficient statistics on the rare nuclei of interest within an affordable experimental time, typically a few days. MINOS comprises a vertex tracker – a Time Projection Chamber (TPC) – placed around the hydrogen target to determine the precise location of P-2P reactions in the target. This information is used to apply the appropriate Doppler effect corrections to improve the resolution of the spectra obtained by the gamma spectrometer surrounding MINOS. The combination of MINOS and a gamma spectrometer (e.g. the DALI2 device available at RIKEN, Japan) places this experimental setup on the forefront of scientific instruments in its field.

This paper describes the design of the readout system for the TPC of MINOS and presents its main features and performance. After a description of the data acquisition chain, we report the experience we accumulated on the exploitation of this system during the four physics campaigns that have been conducted with MINOS at RIKEN.

II. Outline of MINOS Target and TPC

A cutaway view of the central part of MINOS is shown in Fig. 1. The field cage of the TPC is 180 mm in the outer diameter and 300 mm in length. The Micromegas readout plane is segmented in 18 rings of pads of ~2 mm × ~2 mm. Because all pads have approximately the same size, the central ring has only 144 pads while the outer ring, which has the largest diameter, is segmented into 256 pads. Space constraints near this detector necessitated the development of an advanced cabling solution based on sub-millimeter pitch (0.4 mm) micro-coaxial cables to connect all pads to the preamplifiers placed approximately one meter away. Using this technology, tests in experimental conditions show that channel noise remains low, typically ~1500 electrons rms. The measured noise of the readout electronics without cable and detector is of the order of ~800 electrons rms.

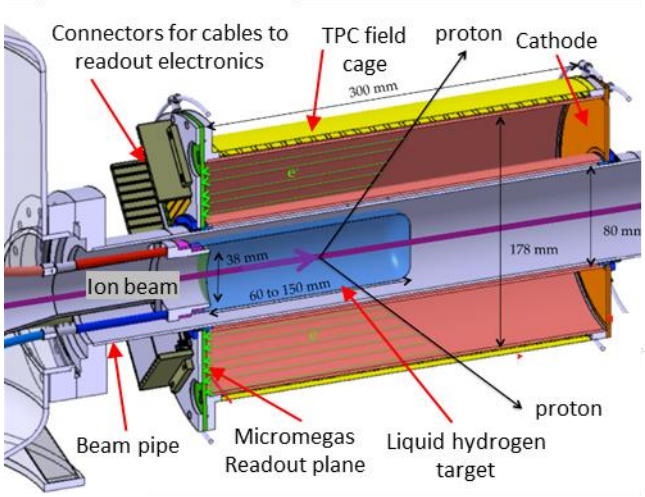

Fig. 1. Cutaway view of the MINOS liquid hydrogen target and TPC. This apparatus is normally installed in a gamma spectrometer, for example DALI2. The protons ejected by the collisions of beam ions on the target produce ionization electrons in the gas of the TPC. The electric field created by the voltage applied on the cathode makes these electrons drift towards the Micromegas readout plane where they are amplified and collected by small pads. Each of the ~3600 pads of the readout plane is connected to an electronic channel via a ~80 cm long micro-coaxial cable.

III. The Readout System of MINOS

A new readout system was designed for MINOS. Its architecture is shown in Fig. 2. A complete description can be found in [2].

A. Front-End ASIC

The built-in versatility of the readout system of MINOS allows exploiting a legacy readout chip, the AFTER [3] designed for the T2K neutrino oscillation experiment, and its pin-compatible evolution, the AGET [4], made for active target

Manuscript received May 30, 2016. This work was supported in part by the European Research Council, ERC Starting Grant agreement MINOS-258567. Authors are with Institut de Recherche sur les lois Fondamentales de L'Univers (Irfu), CEA Saclay, 91191 Gif sur Yvette Cedex, France (telephone: 33-1-6908-6909, e-mail: denis.calvet@cea.fr).

978-1-5090-2014-0/16/$31.00 ©2016 European Union

TPCs. Both of these multi-channel ASICs (72 in AFTER, 64 in AGET) are based on a 512 cell switched capacitor array (SCA). They support a sampling rate up to 100 MHz.

One of the major improvements of the AGET compared to its predecessor is that it includes a discriminator for each channel. The resulting information can be used to elaborate a self-trigger signal. It is also exploited by the chip itself during readout to time multiplex towards the external ADC only the cells corresponding to hit channels. This selective digitization brings a first level of data reduction and substantially cuts dead-time when occupancy is low, because only a small fraction of the SCA matrix is read out.

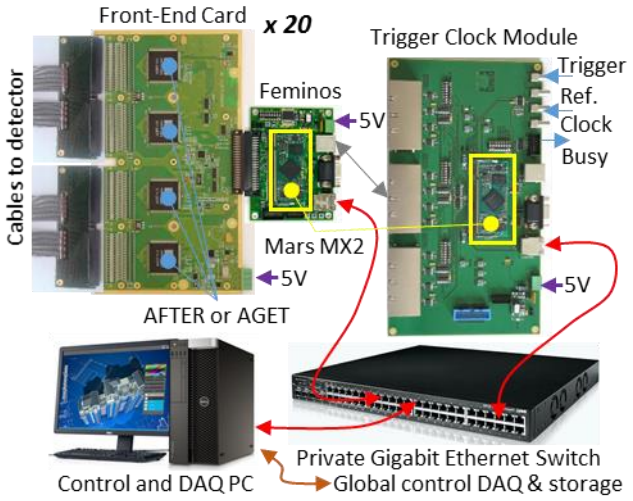

Fig. 2. Architecture of the readout system of MINOS TPC.

B. *Front-End Card*

Two versions of front-end cards (FECs) were used in MINOS: legacy FECs designed around the AFTER chip for the T2K experiment were used for the qualification of the TPC during tests performed at HIMAC (Chiba, Japan) in 2013, and newly produced FECs equipped with 4 AGET chips (i.e. 256 channels) instead of AFTER were used for subsequent physics experiments. Re-using an existing and proven front-end card design allowed considerable savings in development time and efforts. Although assuring pin-compatibility between several generations of ASICs may not always be possible, it has a lot of benefits.

C. *The Feminos*

Another key component of the MINOS readout system is the Feminos card, which makes the interface between one FEC and the other parts of the readout system: the Trigger Clock Module (TCM) and the control and data acquisition PC. The Feminos is a card that plugs at the rear of one FEC. It houses an inexpensive commercial FPGA module, the Mars MX-2 [5]. This compact "System-On-Module" comprises a Xilinx Spartan 6 FPGA, an SDRAM, a FLASH memory, a Gigabit Ethernet PHY, and provides over 100 user I/O pins. Using this macro-component led to an extremely fast development time while the full performance of the AFTER and AGET was preserved by a careful partition of tasks between those implemented in the FPGA fabric and those handled by the embedded MicroBlaze processor. Even low-end FPGAs have now reached the level of performance required to handle data at multi-gigabit per second rates. Although this was not a constraint for MINOS, commercial FPGA-modules generally cannot operate in a magnetic field because they include magnetic parts.

D. *Trigger/Clock Distribution and Data Acquisition*

The readout system of MINOS uses two separate networks: a proprietary fanout network for synchronization and a standard private Ethernet network for configuration and data acquisition. The TCM is a board dedicated to the distribution of a 100 MHz reference clock and the fanout of synchronization signals to all Feminos (e.g. trigger and timestamp reset). It also combines the individual "busy" signal of each Feminos to make a global "Busy" signal indicating that the system is in dead time and cannot accept a new trigger. The TCM controls up to 24 Feminos connected in a star network topology by category 6 RJ45 cables. A proprietary serial protocol is used to transport synchronous messages over DC-coupled LVDS cable pairs. Encoding is selectable between DC-balanced and non-DC balanced.

IV. Experience Return

We present in this section some of the difficulties we had during the exploitation of the readout system of MINOS and explain how these were solved.

A. *Trigger and Clock Distribution Network*

The clock and trigger distribution network was generally stable, sometimes during several days, but in some cases, a slip of one clock period appeared randomly on some Feminos. Currently, the slack blocks the DAQ because the timestamp of the various fragments of the same event do not exactly match. An insufficient time margin, a drift of component characteristics with temperature, or some strong electrical perturbation could be the cause of this problem. Using DC-coupled lines between the TCM and Feminos may also be inferior to AC-coupling to achieve low bit error rate. Finding the exact origin of this issue seems unpractical and we have no other choice than use the current hardware. For the next experiments with MINOS, the event builder software has been changed to tolerate timestamp mismatches between event fragments of one or a few units. Events with a slight timestamp mismatch will be recorded and marked with a special flag. The DAQ will only stop in case of more severe irrecoverable errors.

B. *Event Builder*

Communication between the Feminos and the DAQ PC occurs through a commercial Gigabit Ethernet switch and uses the UDP-IP protocol. We implemented a flow control mechanism in software to guarantee that, globally, all Feminos never send more data than the Ethernet switch and DAQ PC can buffer. Event building tests using 24 Feminos were run stably during many hours at the maximum speed of the Gigabit Ethernet link of the DAQ PC (i.e. ~120 MByte/s). No data loss was observed. During experimental runs, the network load

situation was much more favorable because the average data throughput of MINOS was only a few MBytes/s.

C. Grounding and Electromagnetic Compatibility

Grounding and electromagnetic compatibility are certainly aspects that we failed to anticipate at the design phase. Unwanted ground paths are present through the mechanical support structure of MINOS. Although this oversight had no real impact, it was a serious warning and this negligence is not to be reproduced in other future projects.

During the first tests of the TPC, high voltage sparks on the cathode created perturbations that corrupted the volatile configuration memory of the FPGA of some Feminos. Our control software does not provide the capability to read back and verify all the settings of the front-end electronics after the initial configuration phase. However, it was found sufficient to verify the content of only one configuration register in each Feminos to probe for errors. After analyzing the problem, we found that the power-enable circuit of the main voltage regulator of the Feminos was too sensitive to external perturbations. This problem was corrected by adding a stronger pullup resistor and a filter capacitor to the appropriate control pin. We also re-designed the cathode of the TPC and we ran it at a safe operating voltage during physics experiments. This completely eliminated the sparks that we had during the qualification tests of the TPC.

D. Low Voltage Power Distribution

The FEC and Feminos take 2 A from a 5 V power supply. The readout of MINOS TPC requires 20 FECs and Feminos leading to a total power of 40 A / 5 V, i.e. 200 W. We use standard PC ATX power supplies mounted on custom made support plates. We found that some models generate lots of perturbations on the very sensitive front-end electronics, but many models are just as good as significantly more expensive laboratory equipment.

E. Dead-time Reduction

Reaching a low readout dead-time was a critical requirement for MINOS. The readout time of an individual AGET chip is proportional to the number of channels hit. The readout time of an event in a system that contains several AGET chips is determined, for each event, by the AGET chip that had the highest number of channels hit. To reduce dead time, we designed the mapping of detector channels to front-end electronics so that the hits of the expected tracks (radial most of the time) are spread on different readout cards and AGET chips. This method is very effective, and in practice we observe that typical tracks hit only 3 to 5 channels in an AGET chip. However, we observed during the first experiment with MINOS that some electrical perturbations can trigger all the 64 channels of an AGET chip, causing a very long readout time for these events. The AGET chip uses the so-called “Hit Channel Register” to determine which channels of the SCA matrix have to be read out. Upon trigger, the content of this register is latched. The hit pattern can be read by the device controlling the AGET, but it can also be altered to define exactly which channels to digitize. We use this capability of the AGET chip to define on the fly which channels are readout. After a trigger, each Feminos reads the Hit Channel Register of the 4 AGET chips it controls and calculates the number of channels hit in each chip. If this number is below a programmable threshold (e.g. 12), the Hit Channel Register of the corresponding chip is not altered. Else, the Feminos clears the Hit Channel Register of that chip, so that it is masked for this event. Using this technique, spurious noise that illuminate an entire chip or one front-end card no longer impacts dead-time.

During one of the latest experiment that was made, the typical average dead-time of MINOS was ~140 µs. This corresponds to ~5 channels hit in average for the busiest AGET chip of every event.

V. Conclusion and Future Work

In a short period of 5 years, the MINOS collaboration has successfully designed, built, qualified and exploited a complete new instrument and readout system. So far, four physics experiments have been conducted with MINOS at RIKEN and new ones are planned.

Besides MINOS, the readout system presented in this paper, or part of it, is used by approximately ten other projects. Although we decided to discontinue the production of the different cards that compose this system, a more compact and improved version is planned to be designed.

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