IRIO TECHNOLOGY: DEVELOPING APPLICATIONS FOR ADVANCED DAQ SYSTEMS USING FPGAS

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  - Advanced applications: using GPUs for ITER diagnostics
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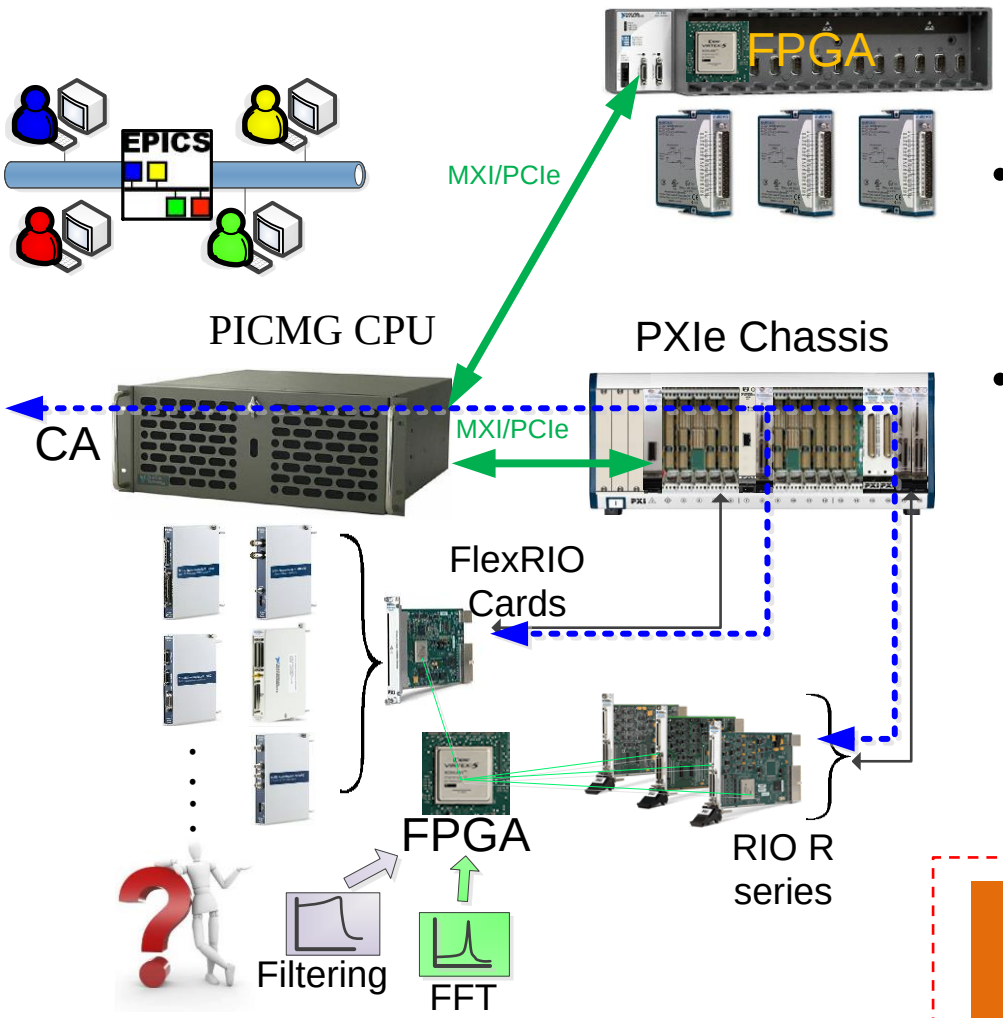
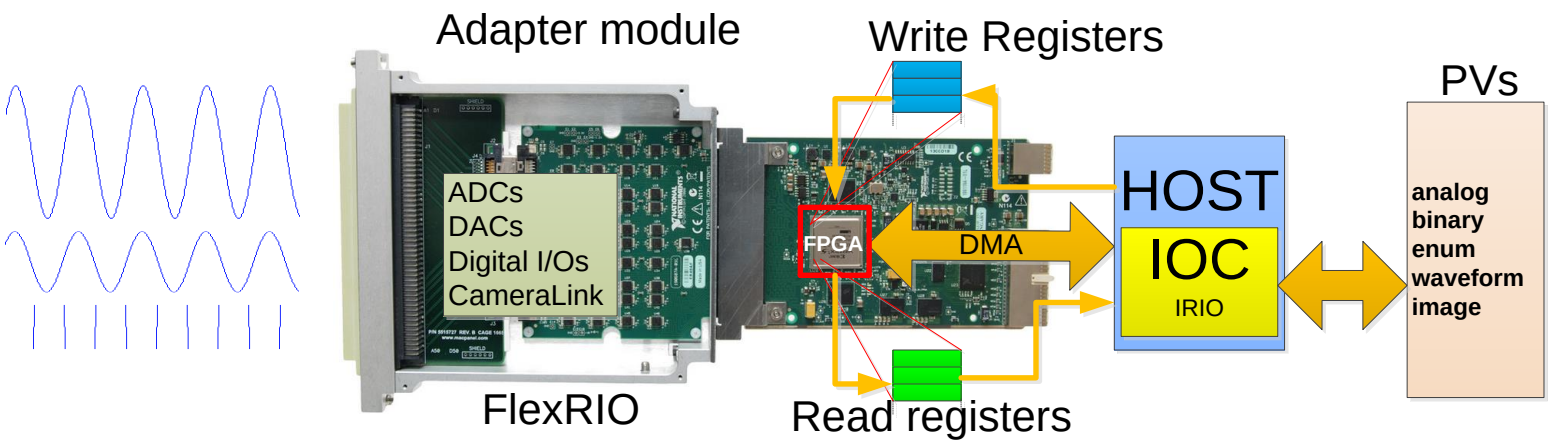
Motivation



- FPGAs provide reconfigurable hardware with deterministic data preprocessing capabilities
- Graphical tools such as LabVIEW for FPGA reduces development and integration time
- The combination of both technologies with EPICS simplifies the development of complex control, data acquisition and processing systems

IRIO is a set of software tools simplifying the integration of RIO devices in EPICS

RIO/FlexRIO Devices



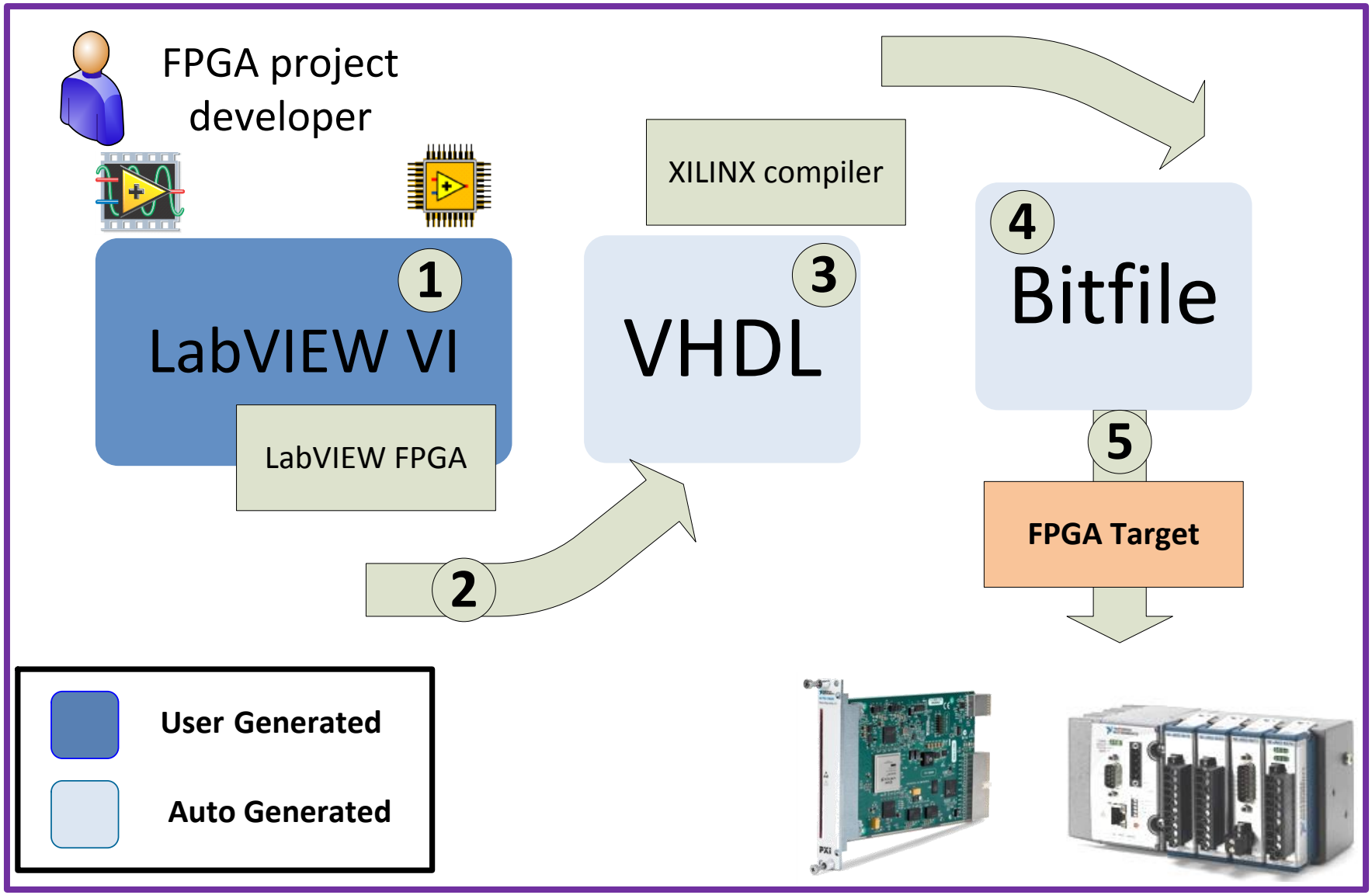
1

The developer defines the functionality programming the FPGA

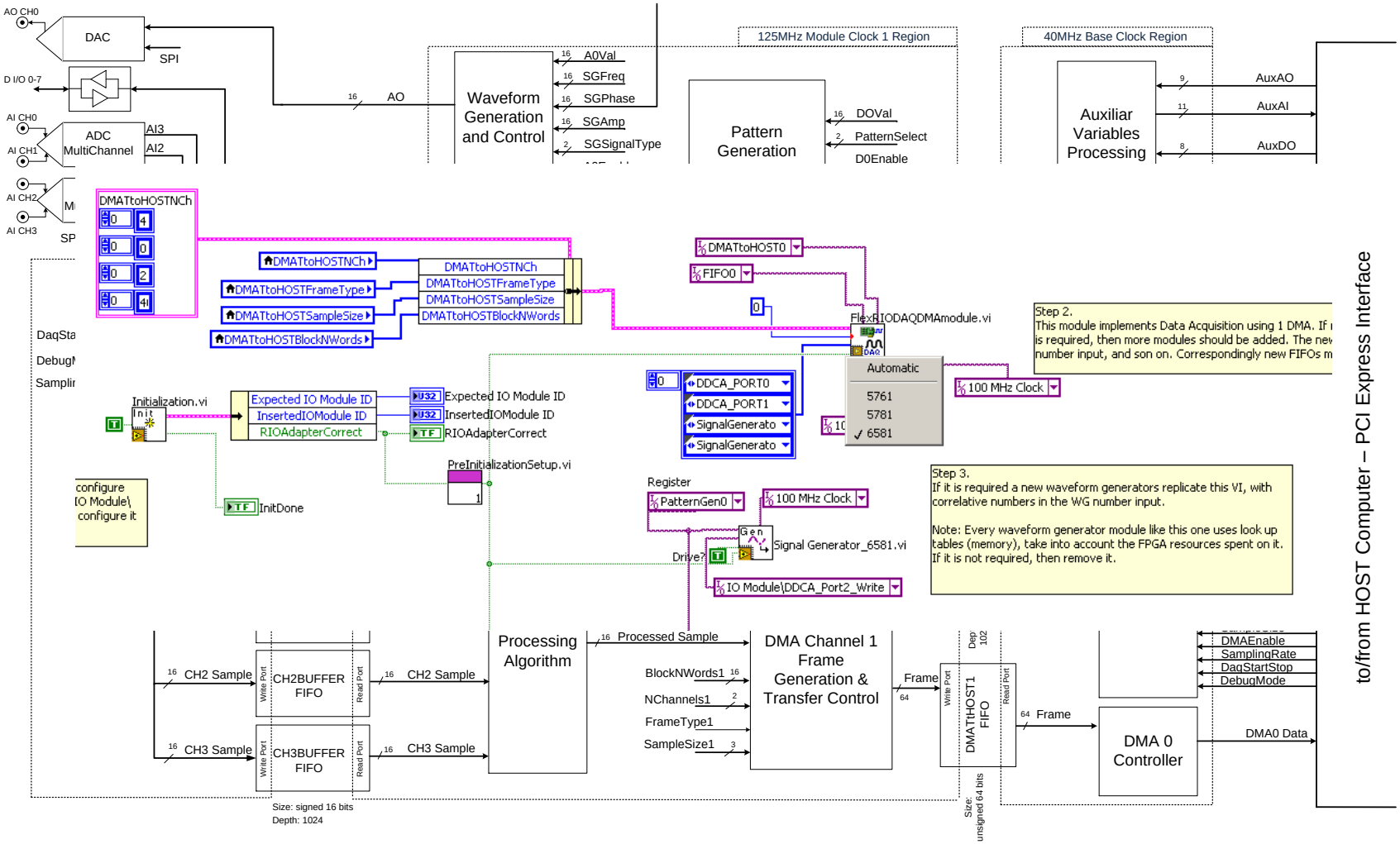
2

EPICS connects a user defined device with PVs for configuration and supervision

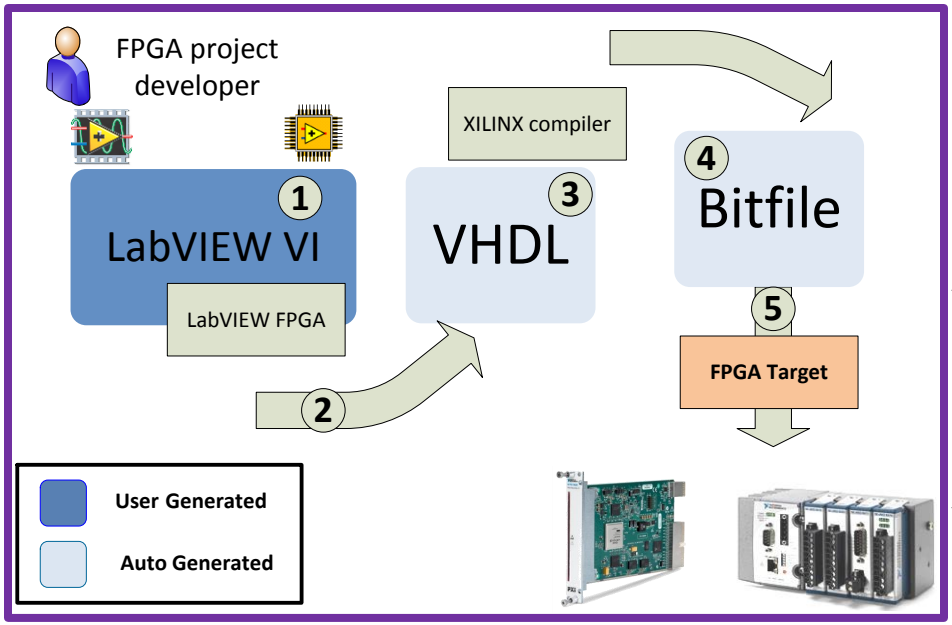
Development cycle: LabVIEW for FPGA

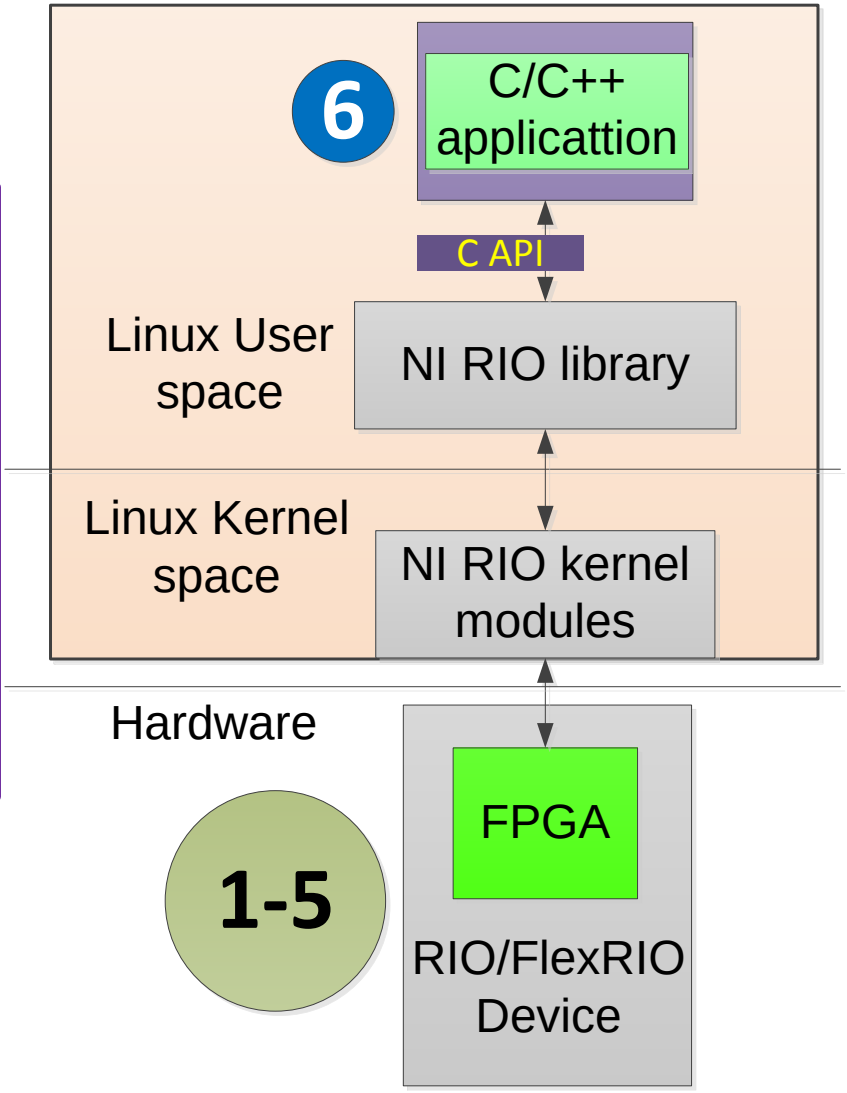


Reducing development time in FPGAs using templates

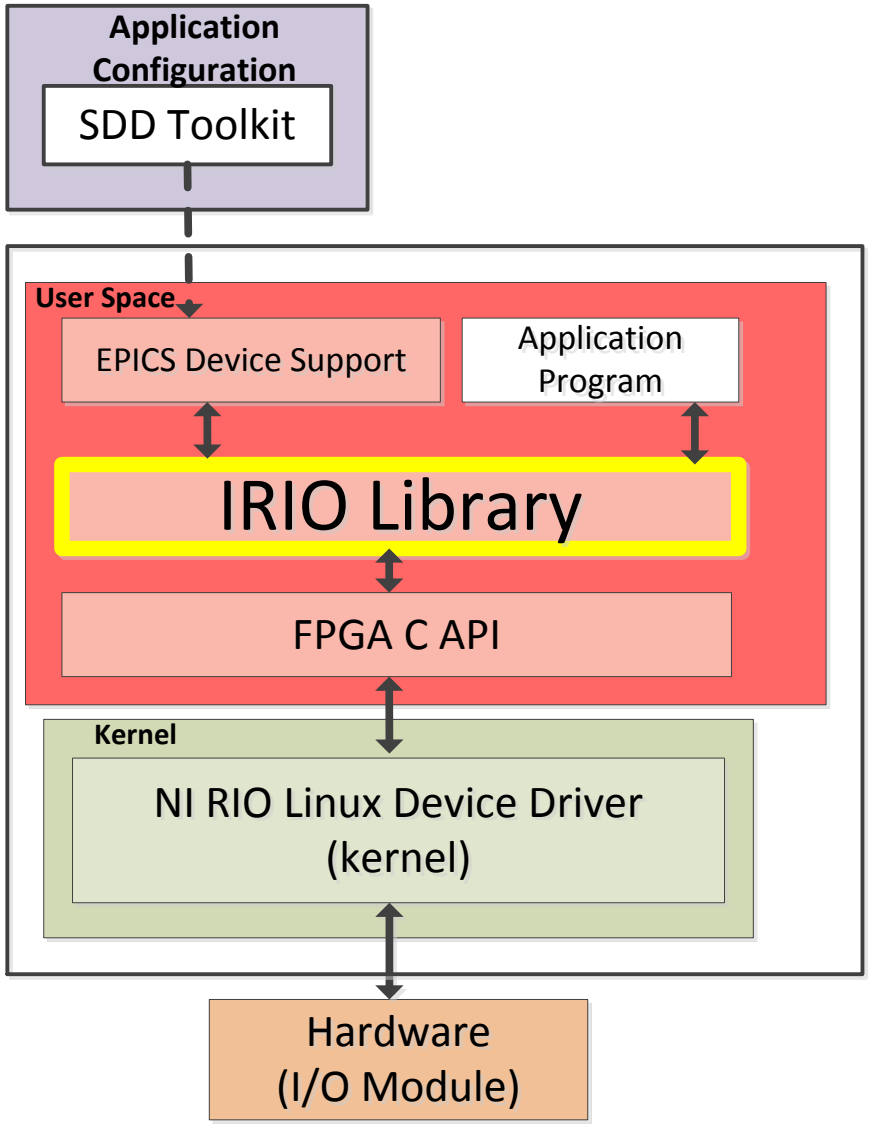


Using RIO devices in Linux



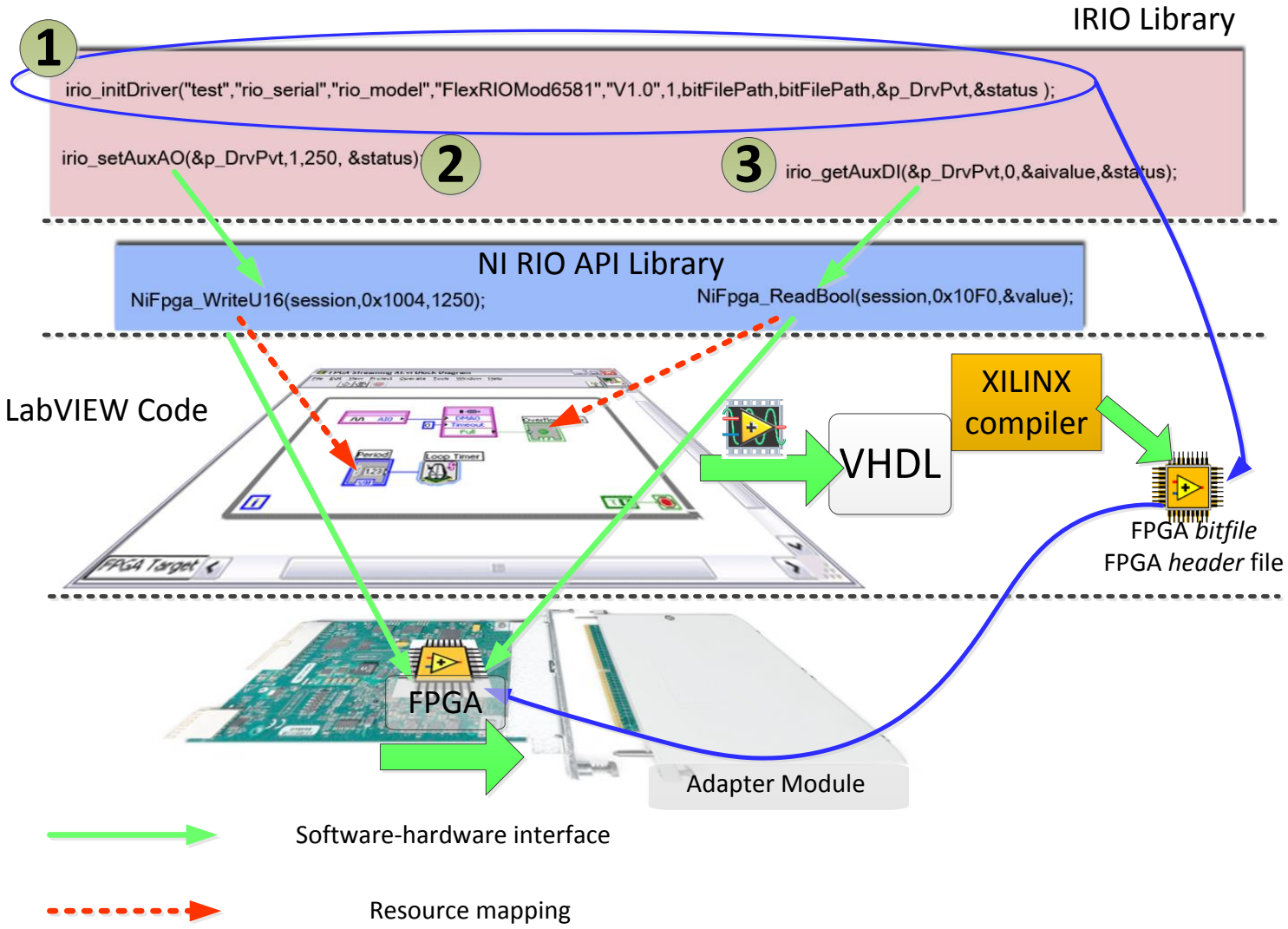


IRIO Project: IRIO Library

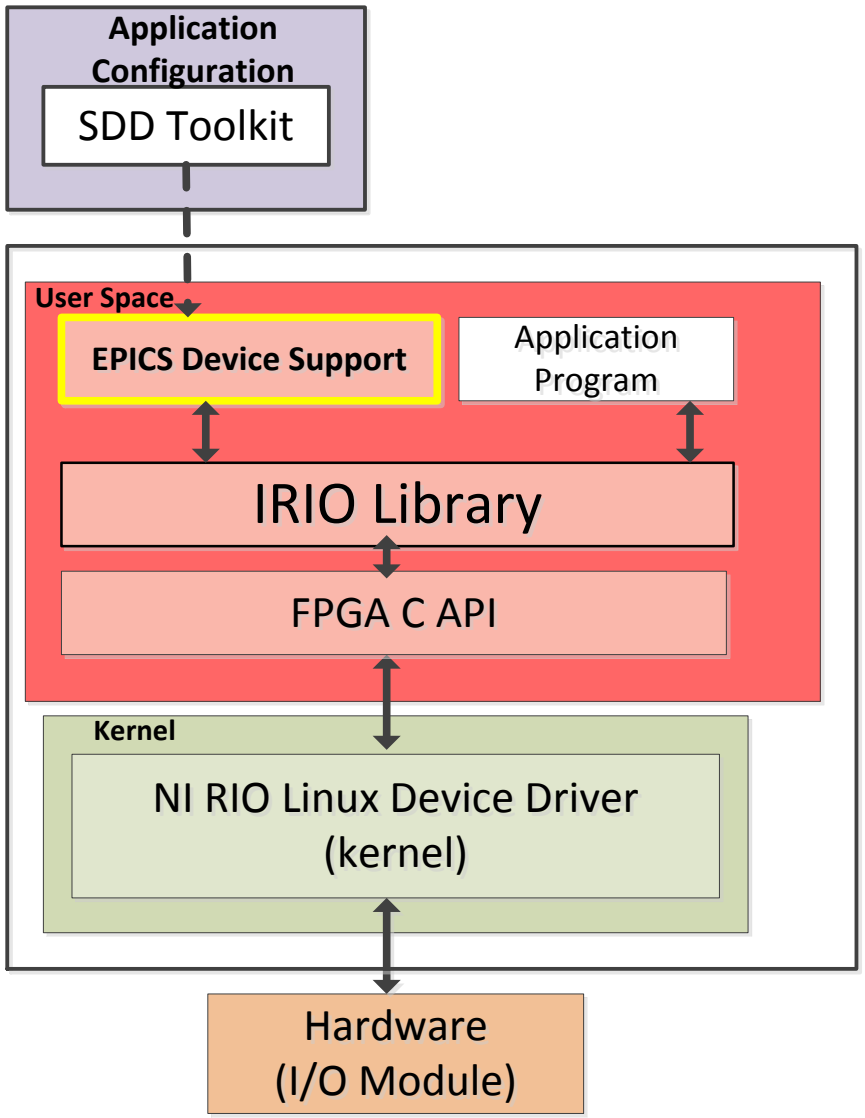


- Identification of the resources implemented in the FPGA
  - The Design Rules document describes the rules for the FPGA implementation
- Provides an API simplifying the interface with the FPGA.
  - Access to FPGA registers
  - Analog input
  - Digital I/O
  - DMA acquisition
  - Image acquisition using cameralink
    - Serial line for camera configuration
  - Signal Generation (DDS)

IRIO resources mapping

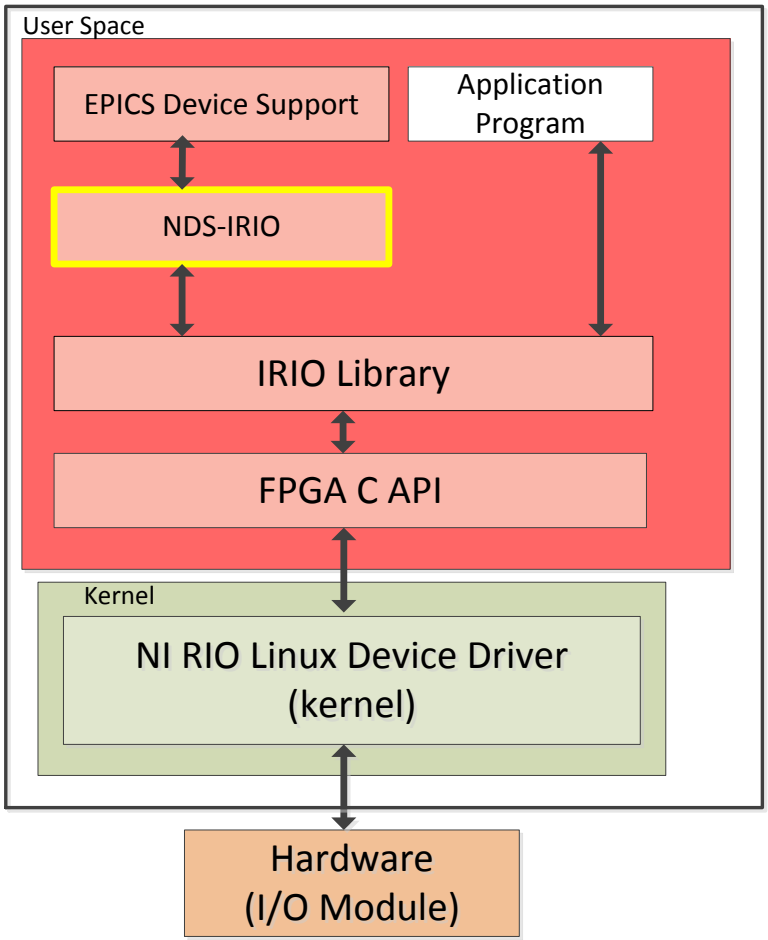


IRIO Project: EPICS driver using asynDriver



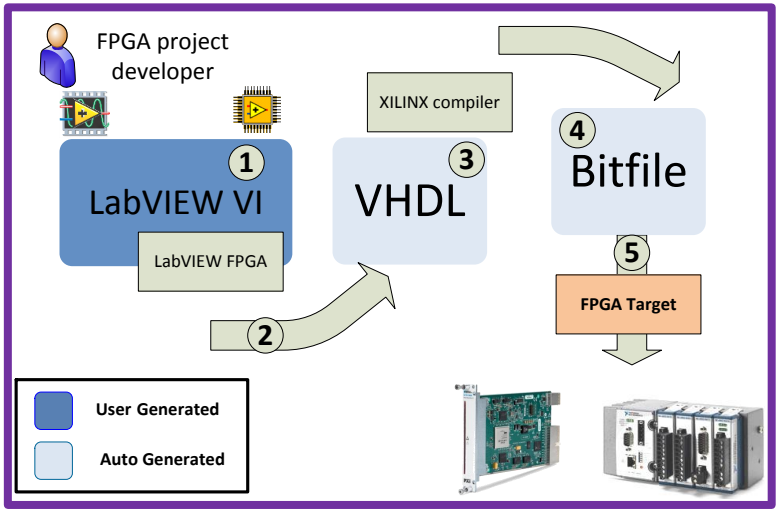
- ✓ EPICS device driver using asynDriver implementation for RIO devices (FlexRIO and cRIO) using IRIO library
  - ✓ Automatically connects the PVs with FPGA resources using IRIO library
- ✓ If the user changes the FPGA design no compilation is needed
- ✓ ITER SDD generates the complete software unit

IRIO Project: C++ classes for Nominal Device Support

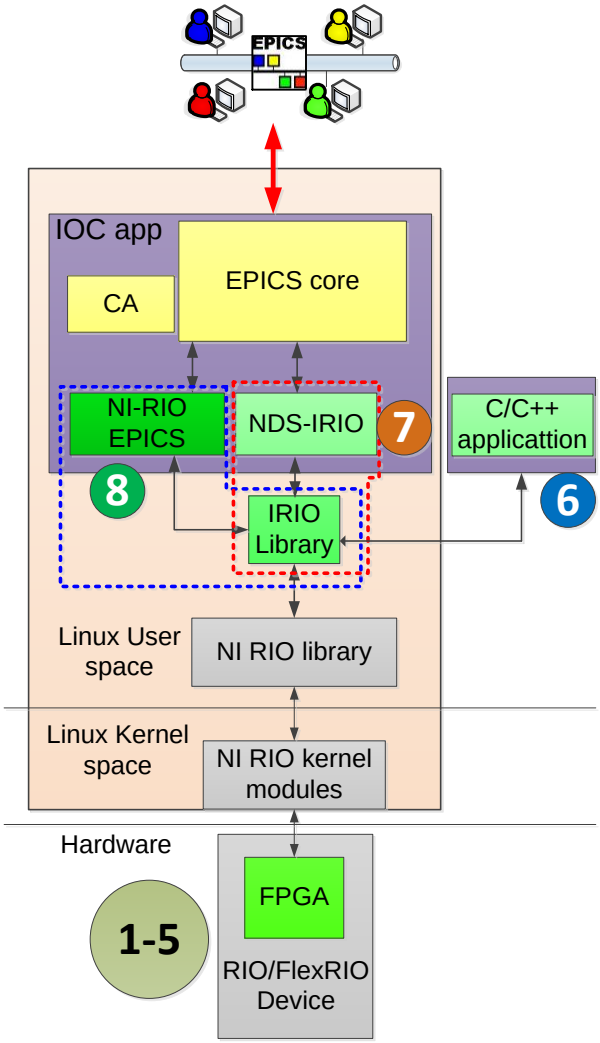


- Nominal Device Support approach defines a set of classes and PVs to be used for EPICS driver implementation.
- NDS-irio is the set of NDS extended classes to use FlexRIO devices
- Simplify the implementation of EPICS device support for FlexRIO using NDS

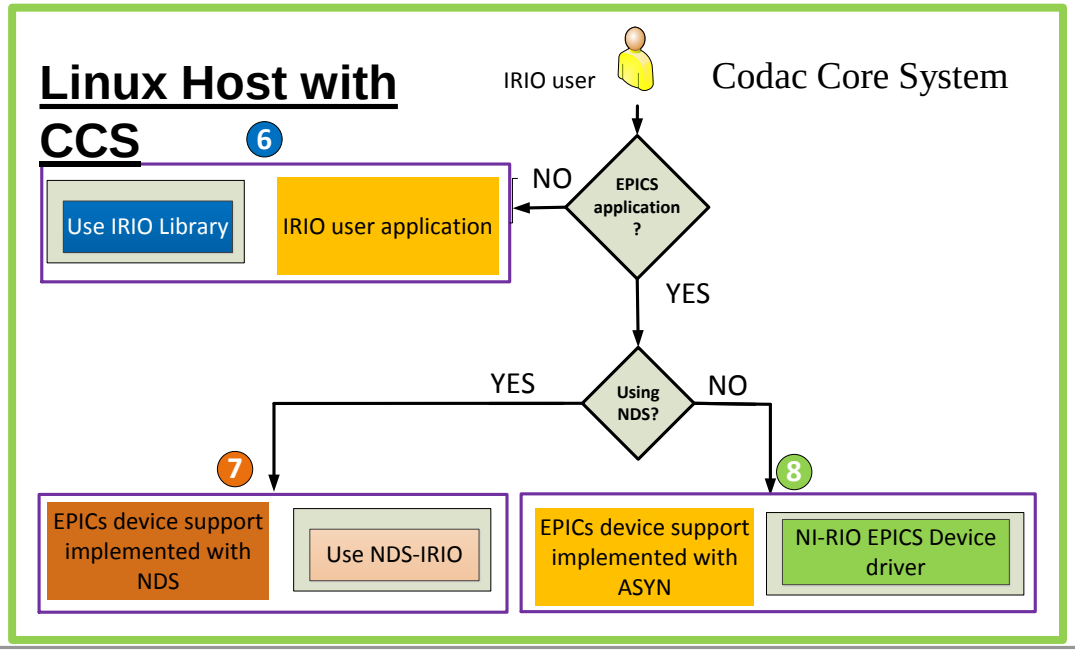
Design Methodology



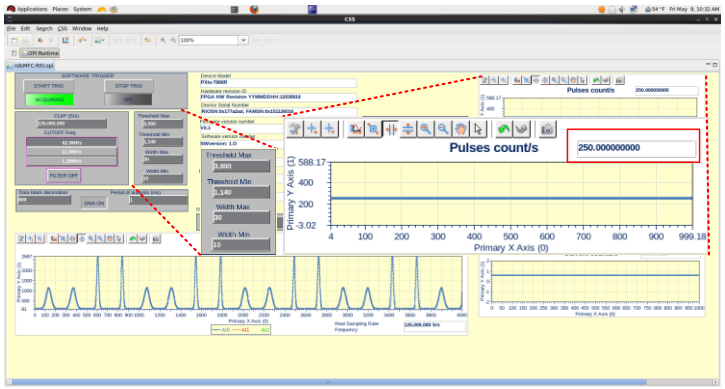
Windows Host

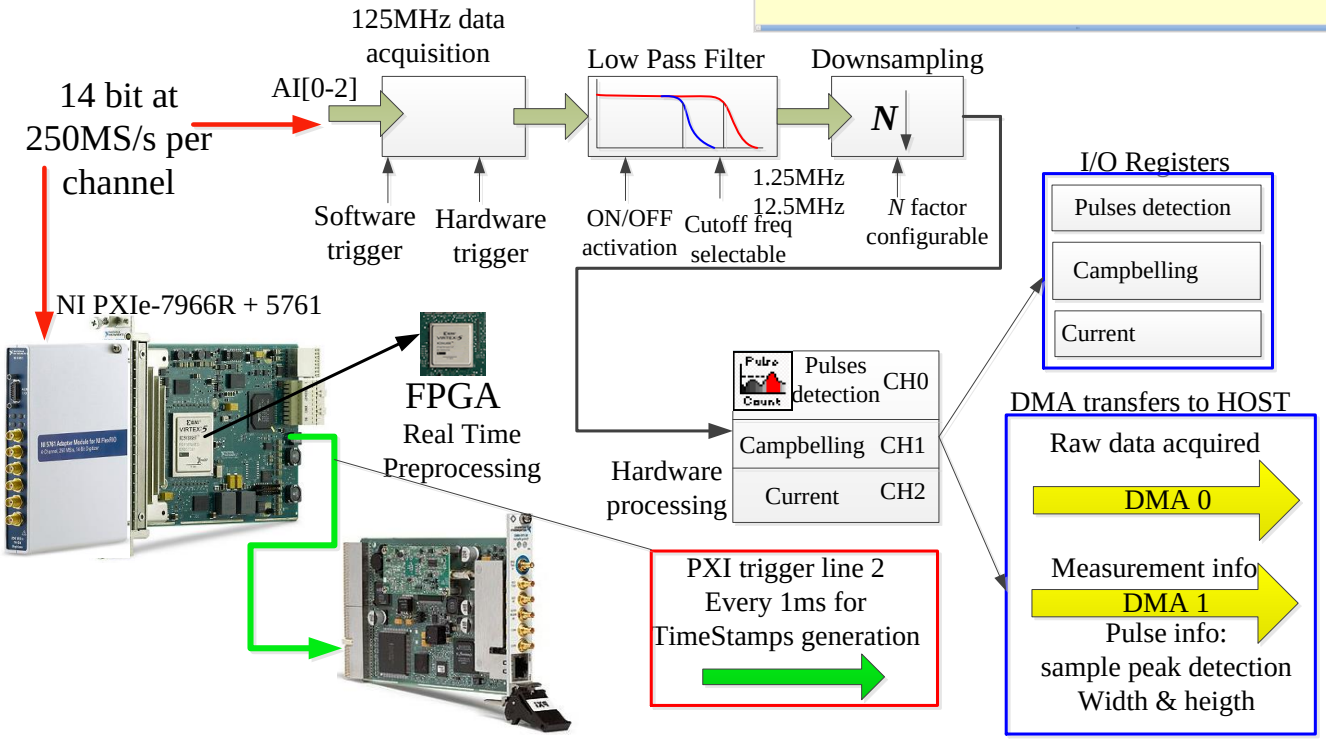


Linux Host with CCS



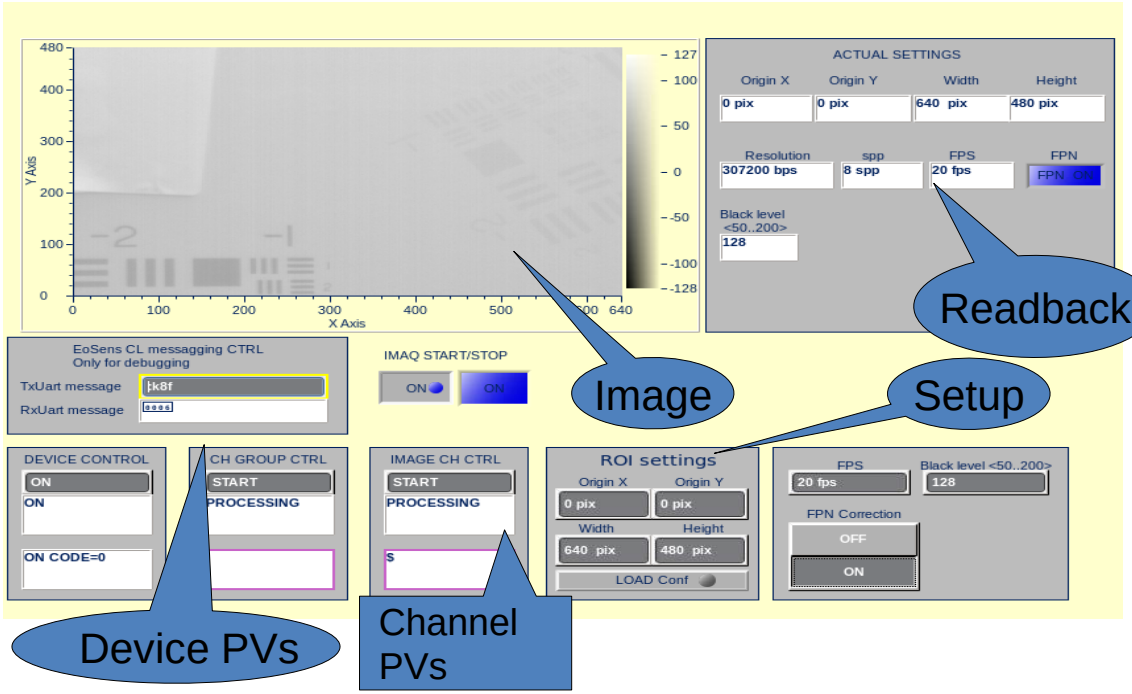
- Integrate deterministic diagnostic into the FPGA (4 ADC sampling at 125MS/s). Data processing to detect/count pulses, RMS, and campbelling





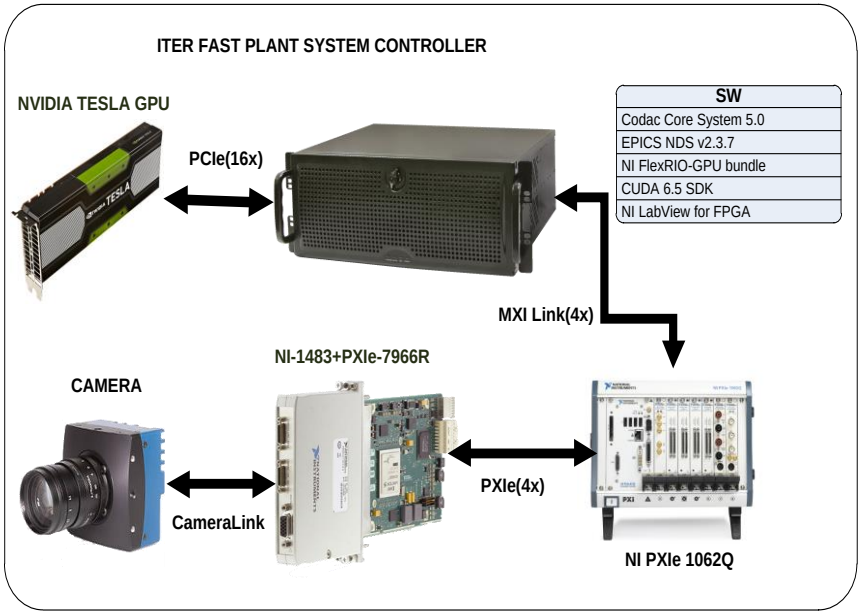
PICMG
Fast Controller
(fc18-3)

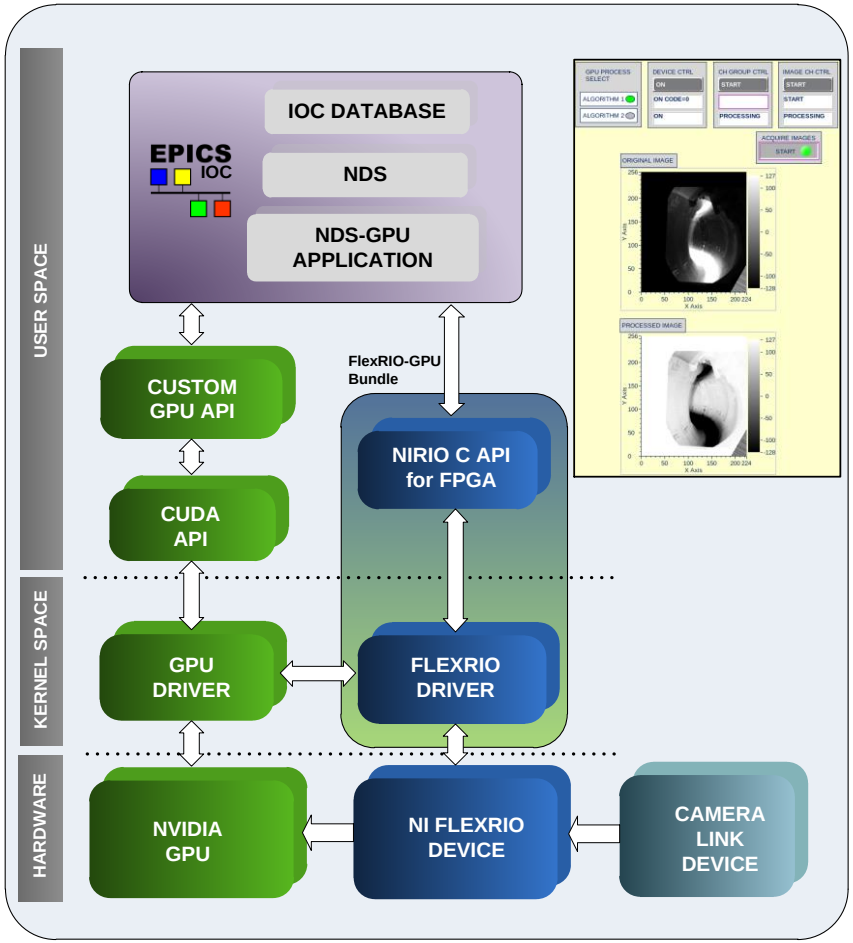
Can we add more processing capabilities?
Is it possible to add a GPU?



FPGA+GPU processing

- NI-RIO Linux Device Driver modified to implement direct DMA from FPGA to GPU





Conclusions

- We have defined a design methodology for implementing advanced data and image acquisition applications with RIO/FlexRIO devices, integrated with EPICS using IRIO software
- We have developed different LabVIEW/FPGA patterns and libraries for RIO devices
- It is not necessary to rewrite or even recompile the EPICS device support for every cRIO/FlexRIO configuration
- IRIO tools integrated in ITER CODAC Core System V5.2 (February 2016)
- IRIO tools are GPLV2
- Current users of IRIO:
  - ITER Diagnostics use cases, KSTAR project, Russian DA (cRIO)
  - ESS Bilbao

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Thank you very much for your attention!!
questions?