A VXS [VITA41] TRIGGER PROCESSOR FOR THE 12GEV EXPERIMENTAL PROGRAMS AT JEFFERSON LAB

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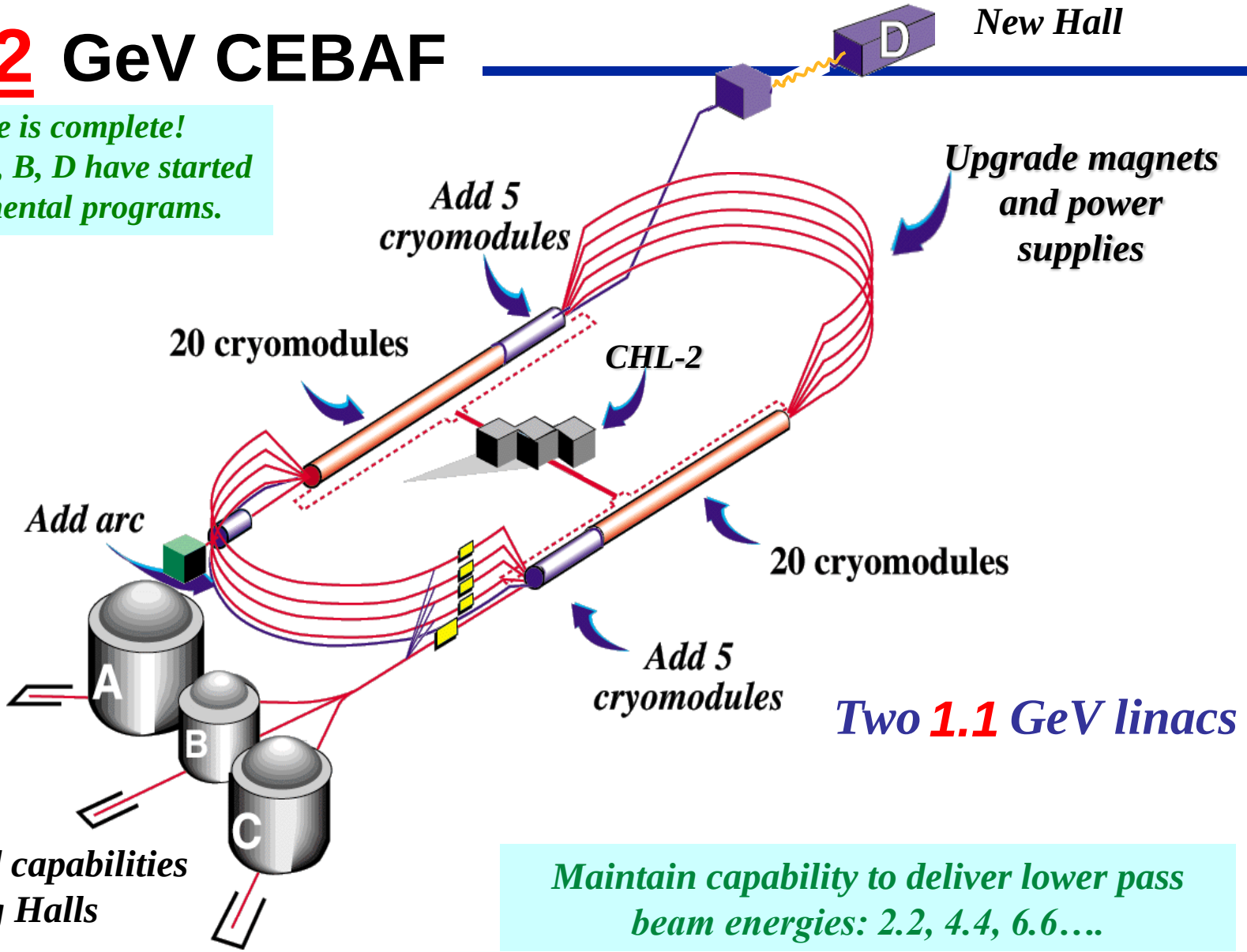
Experimental Nuclear Physics Division

OUTLINE

1. Overview: Jefferson Lab @12GeV
2. 12GeV Trigger Processing System Description
3. 2nd Generation VXS Switch Slot
4. Engineering – Merging the Switch Slot Designs
5. VTP performance and features
6. Summary

12 GeV CEBAF

Upgrade is complete! Halls A, B, D have started experimental programs.



Two 1.1 GeV linacs

Enhanced capabilities in existing Halls

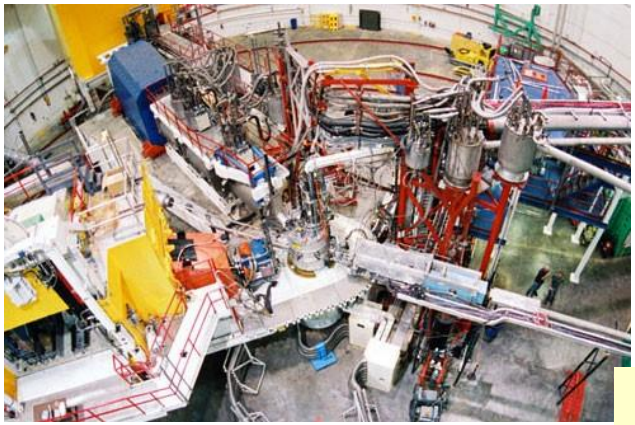
Maintain capability to deliver lower pass beam energies: 2.2, 4.4, 6.6….

New Capabilities In Halls A, B, & C, & New Hall D

9 GeV tagged polarized photons and a 4π hermetic detector

D

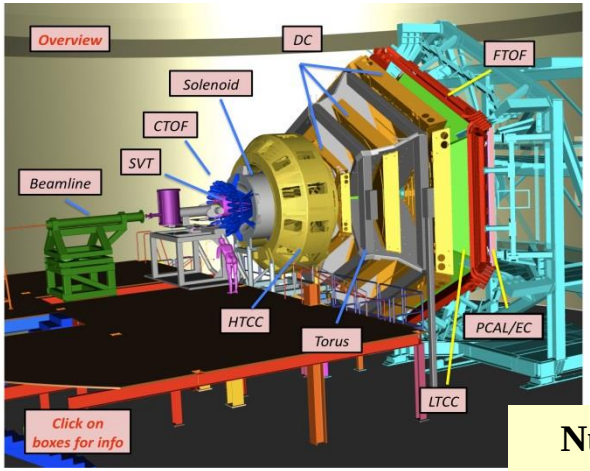
Exploring origin of confinement by studying exotic mesons.



Super High Momentum Spectrometer (SHMS)

C

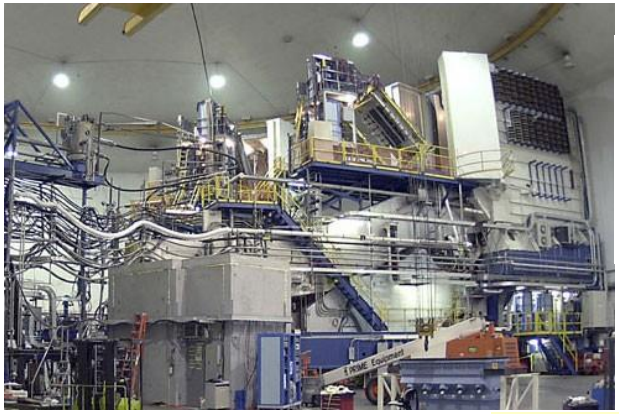
Precision determination of valence quark properties.



CLAS upgraded to higher (10^{35}) luminosity and coverage

B

Nucleon structure via generalized parton distributions.



High Resolution Spectrometer (HRS) Pair, and large installation experiments

A

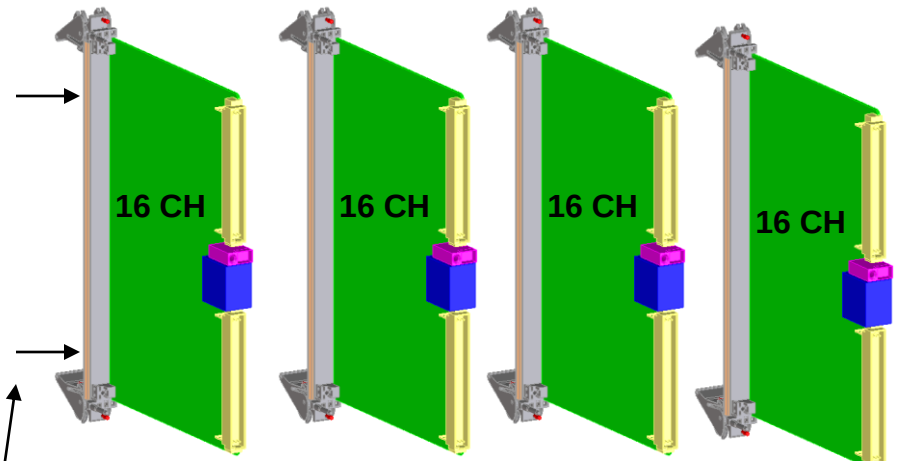
SRC, FFs, Hypernuclear, Standard Model studies (PV, Moller)

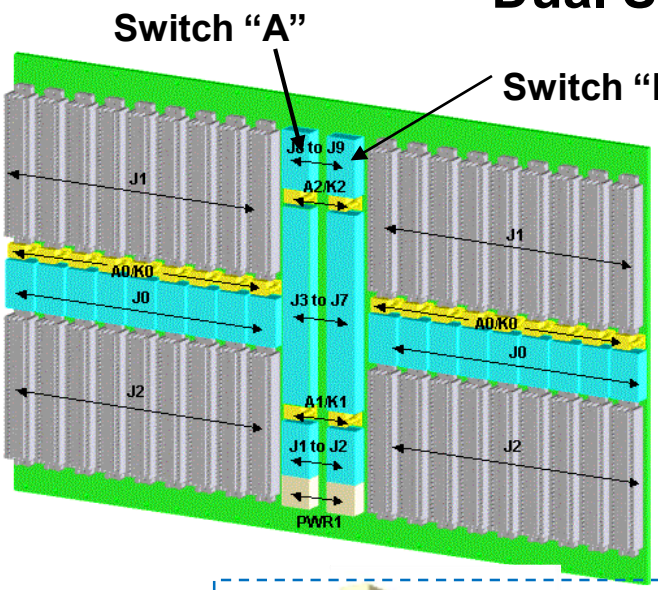
Quick VITA 41 *VXS Review

VXS "Payloads" (JLAB FADC)

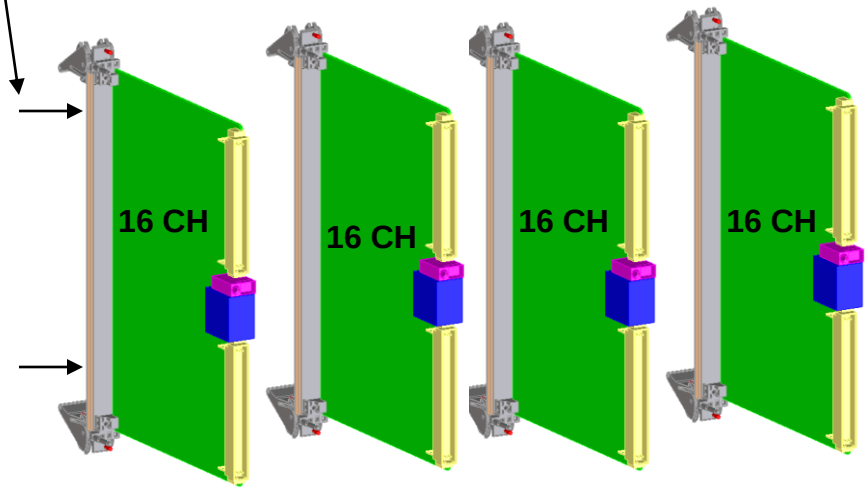
(*VME with Serial Extensions)

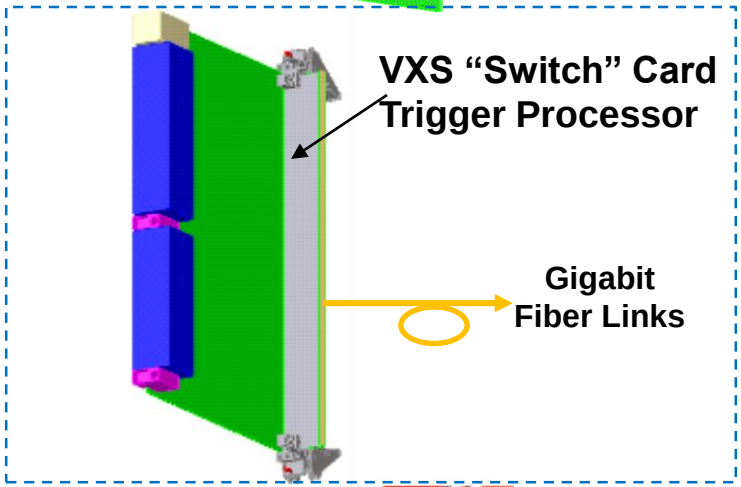
VXS Backplane "Dual Star"



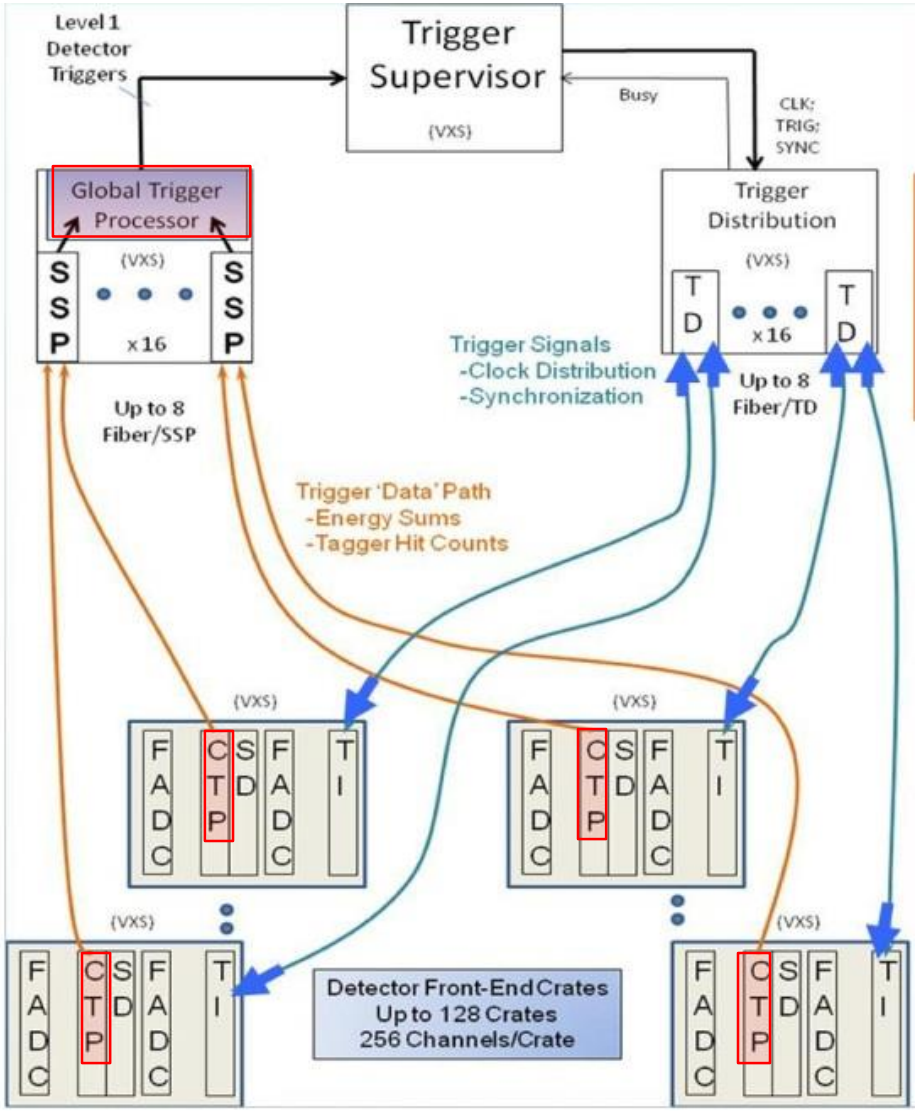


Detector Signals





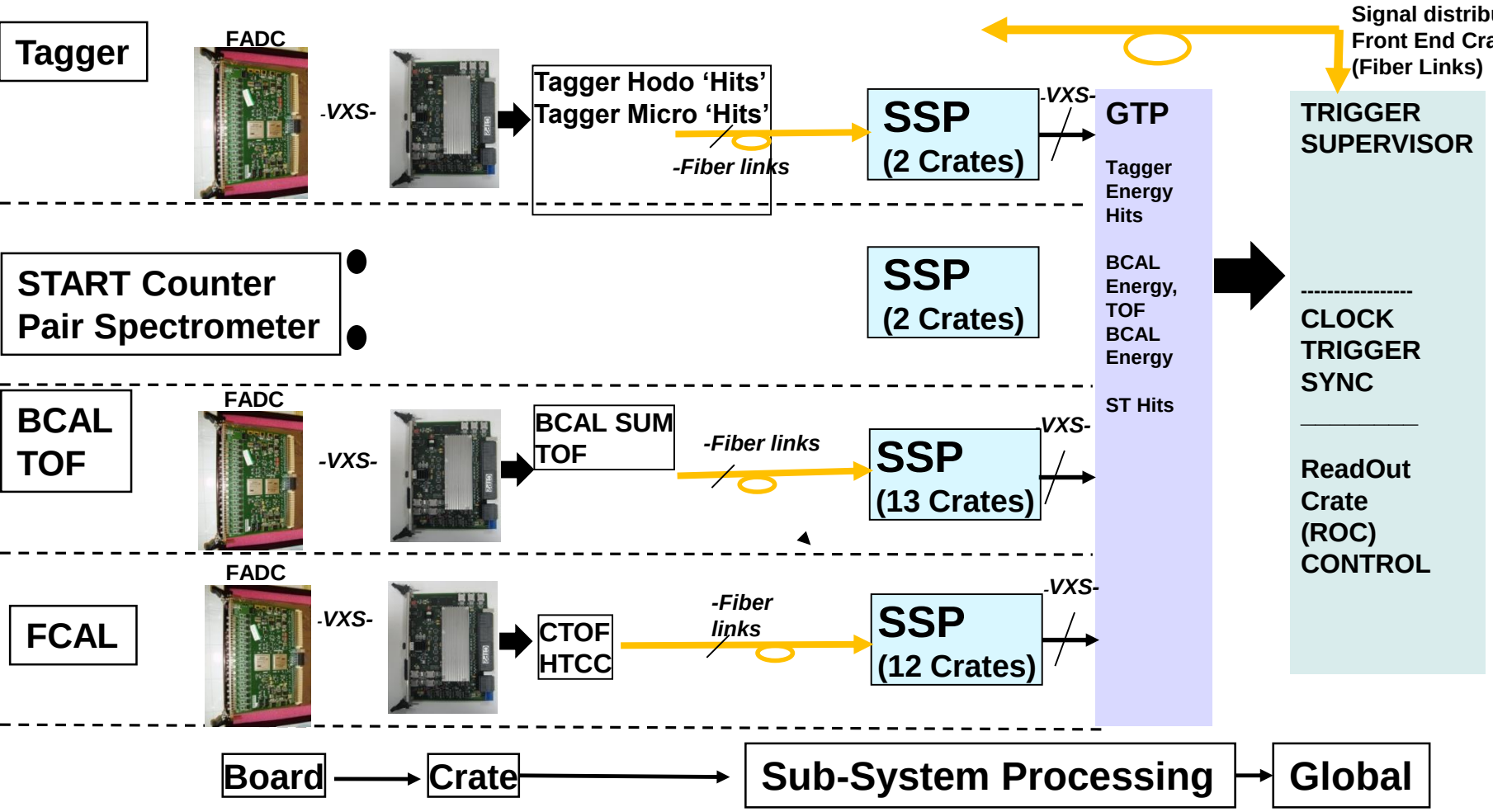
Trigger Processing Implementation – JLAB @12GeV



- **Global Crate**
  - Global Trigger Processor
  - VXS 'Switch Slot'
  - Trigger Supervisor
    - *Clock, SYNC,Trigger

- **Front End Crates**
  - Crate Trigger Processor
  - VXS 'Switch Slot'
  - CPU Readout/Contro
    - Not shown

Hall D Level 1 Trigger



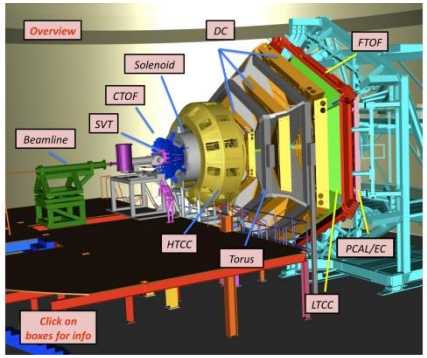
55 DAQ Crates; 30 crates used for Trigger

25-35KHz Trigger Rate

600-700MB/s to Disk; Live time 93%

CLAS12 DAQ Readout Rates

DAQ Module (QTY)	Channel Count	Detector(s)[2]	Raw Data Rate	Triggered Data Rate (@20kHz)
FADC250 (~250) 16 channel, 12bit ADC 250Msps	~4,000	ECAL, PCAL, FTOF, CTOF, HTCC, LTCC, FT, CND	~1.5TB/s	~3Gb/s (no zero suppression, 100ns raw) ~30MB/s* (100ns raw) ~3MB/s* (“fit” pulses)
DCRB (252) 96 channel, amplify/discriminate 1ns TDC	24,192	Drift Chamber	~1GB/s[1]	~20MB/s[1]
VSCM (33) 1024 SVT FSSR ASIC channels	33,792	SVT	~10GB/s[1]	~40MB/s[1]
RICH FPGA (140) 192 channel MAPMT readout 1ns TDC	25,024	RICH	~10GB/s[1]	~20MB/s[1]



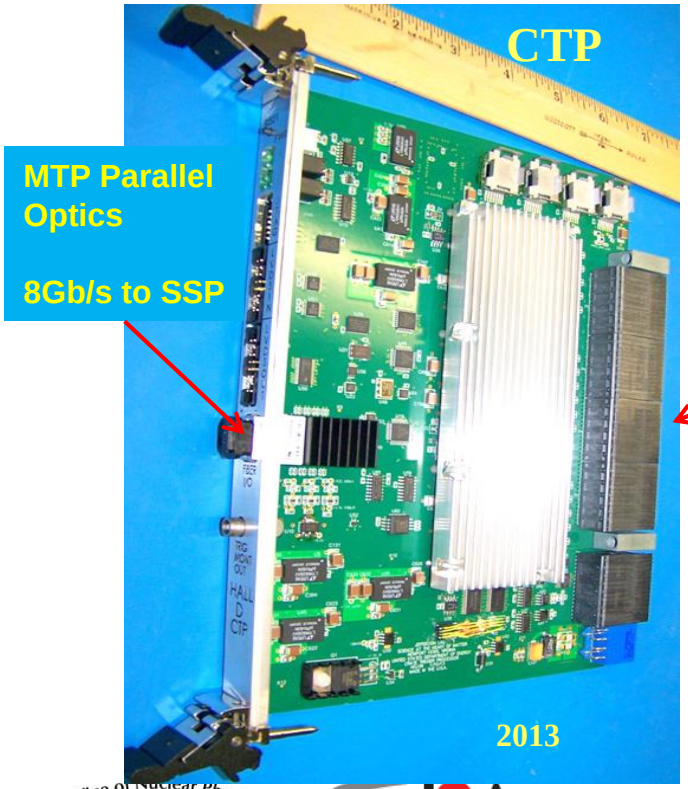
Standard CLAS12 experiments achieve massive data rate reduction in a triggered system (for relatively low trigger rates)

[1] data rate for each 1% occupancy of detector
[2] not all CLAS12 detectors or DAQ modules listed

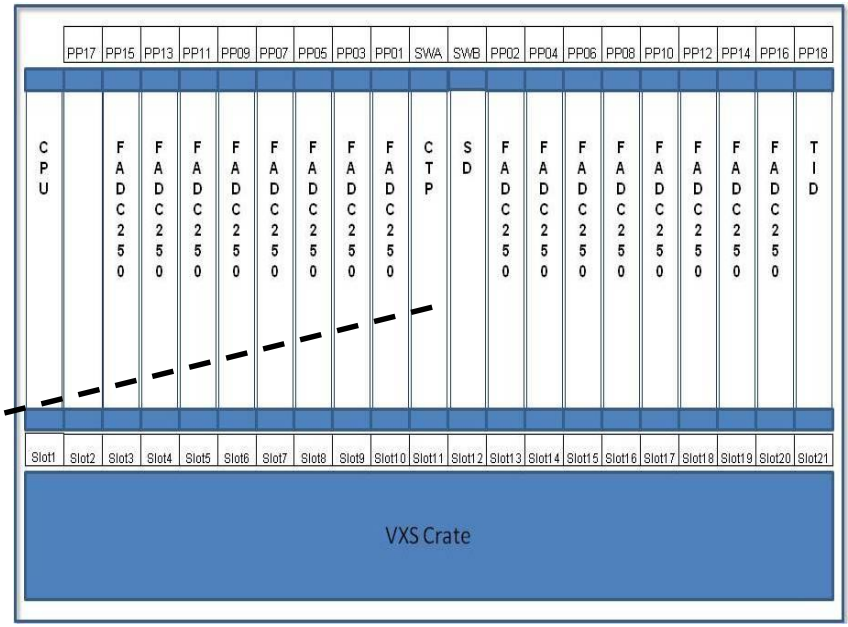
1st Generation Crate Trigger Processor

J. Wilson
H. Dong

- Board includes:
  - 2 VirtexV FX70T
  - 1 VirtexV FX100T
  - 5Gbps link to FX70T on FADC250 boards
- Crate Trigger Processor computes a crate-level energy sum (or hit pattern)
- Computed crate-level value sent via 8Gbps fiber optics to Global Trigger Crate (32bits every 4ns)



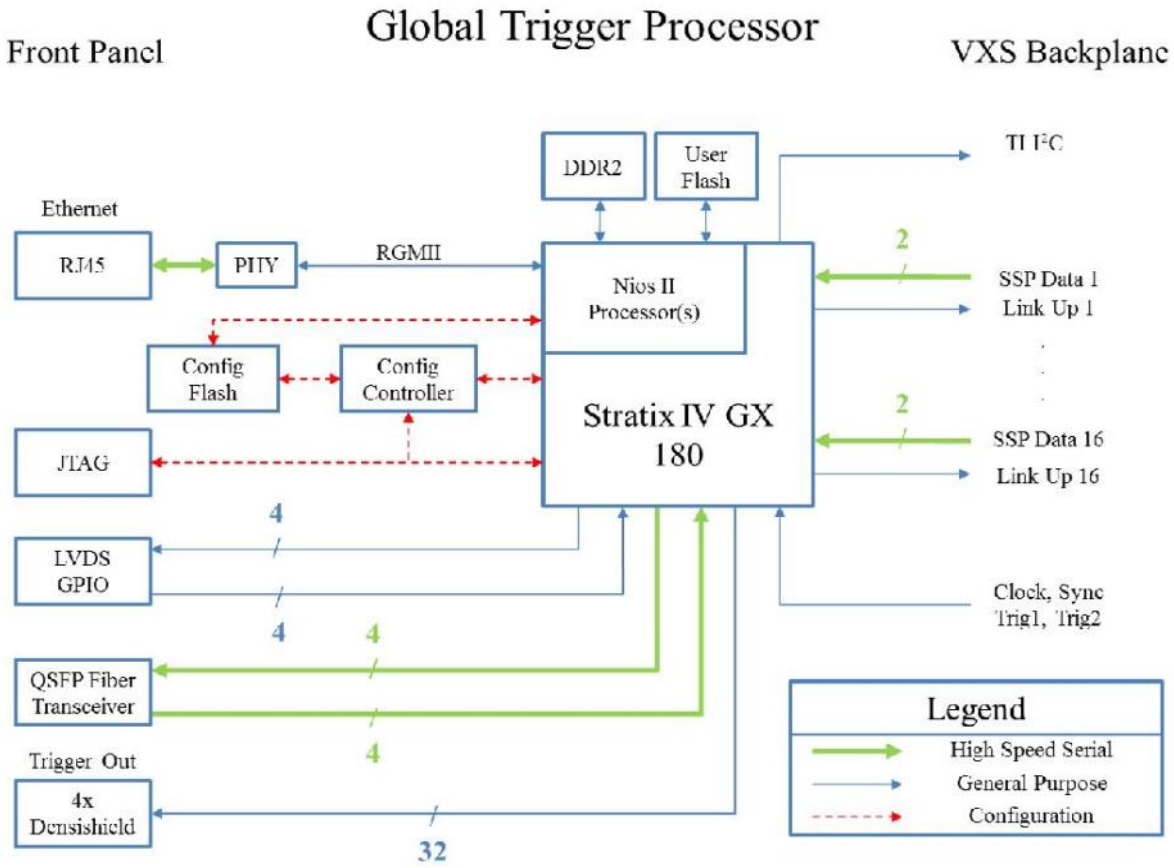
VXS Connectors Collect serial data from 16 FADC-250
2 Full Duplex 'Lanes" @5Gbps



- Control registers read/write via I2^C to VME controller
- No Ethernet interface

- Hall D uses 25 units
- Hall B requires 38 units

1st Generation Global Trigger Processor

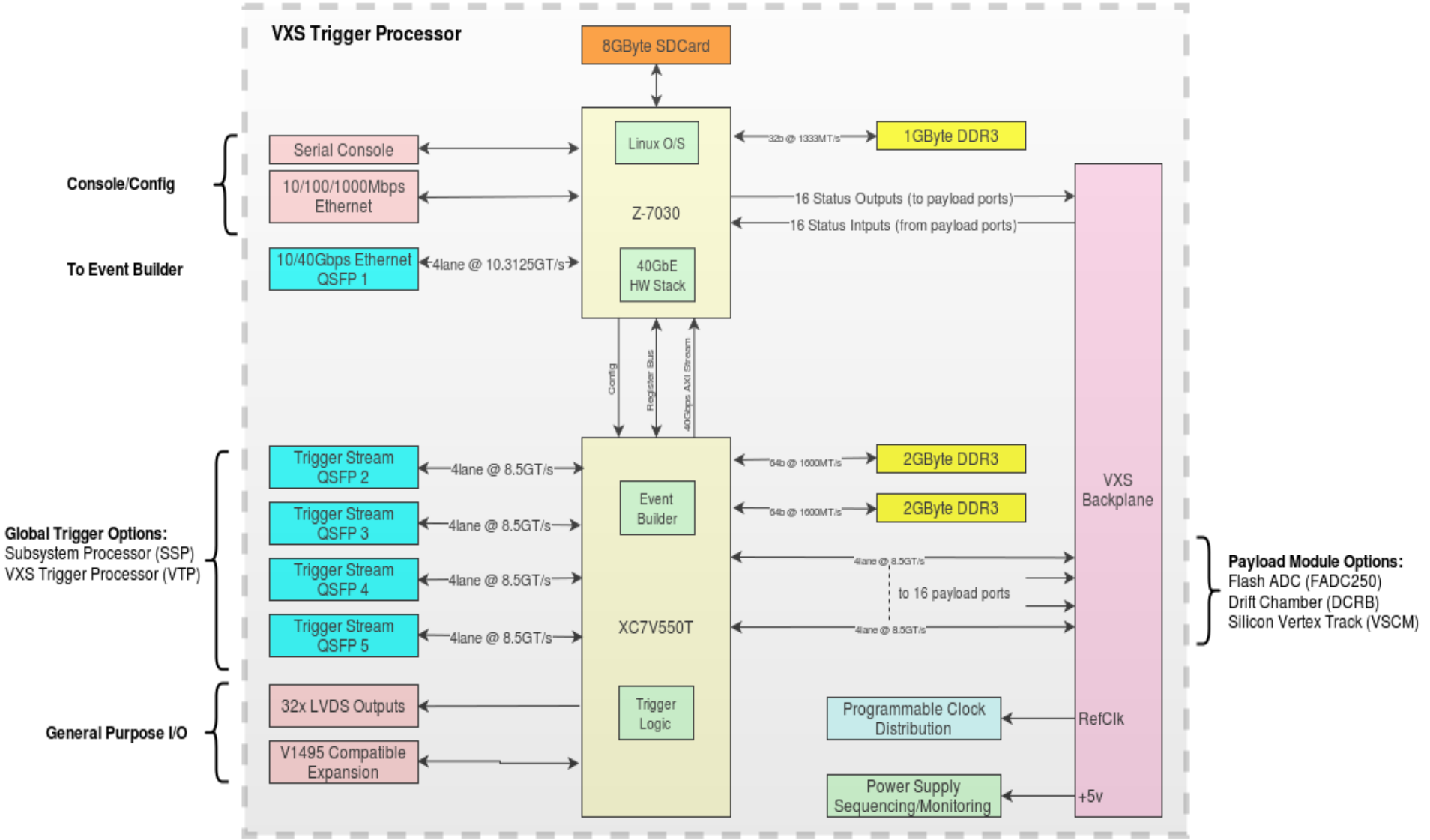


- I^2C to VME controller
- 1Gb Ethernet – Front Panel
- Linux OS (Altera NIOS)
- 1 board per Hall
  -Top Level Trigger Device

- 32 LVPECL outputs to Trigger Supervisor (Densi-shield connector
- 2 x 5Gbps VXS interface (Aurora)

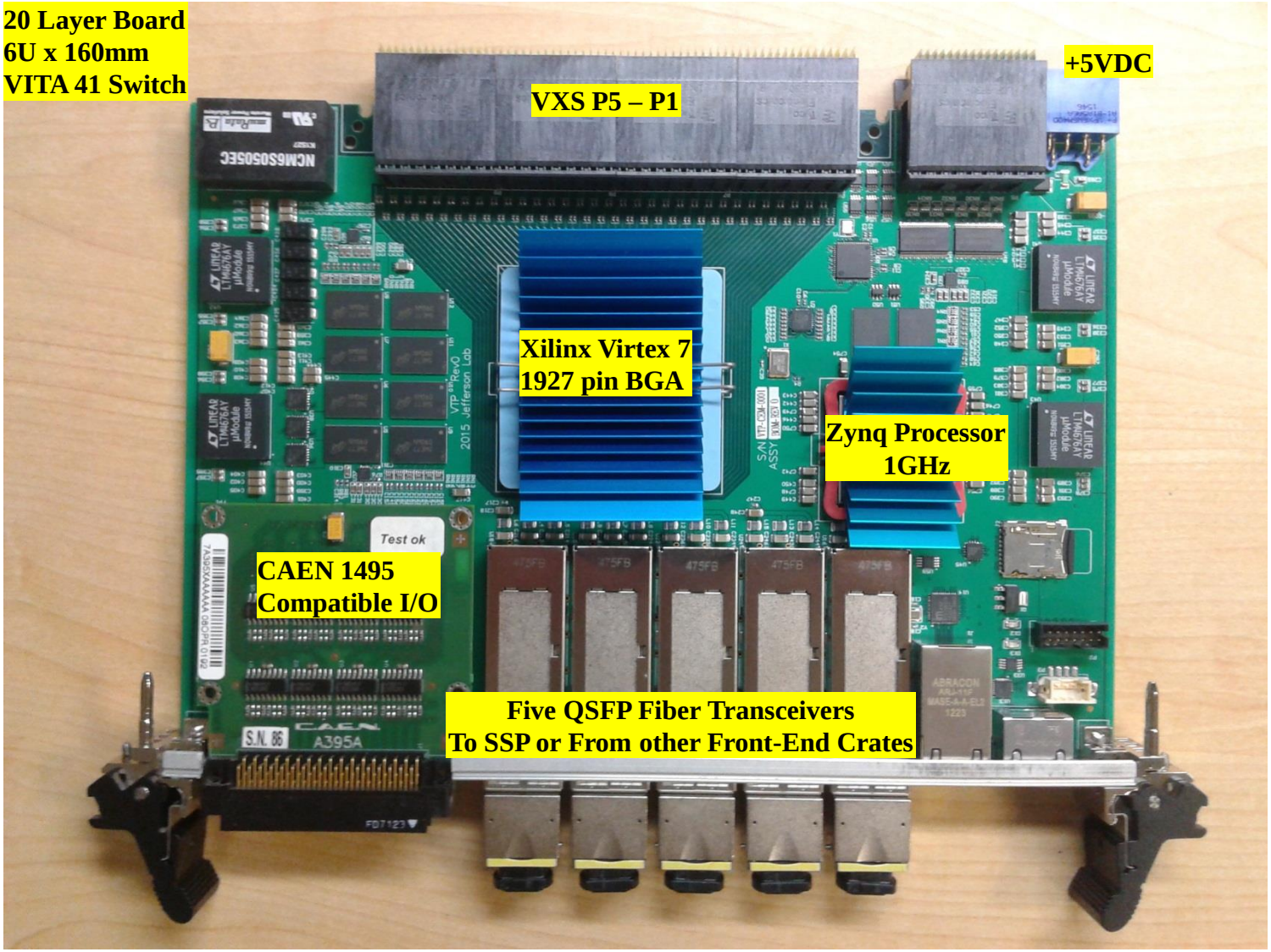
Merging Designs {CTP + GTP}→VTP Logical Diagram

B. Raydo
J. Wilson
C. Cuevas

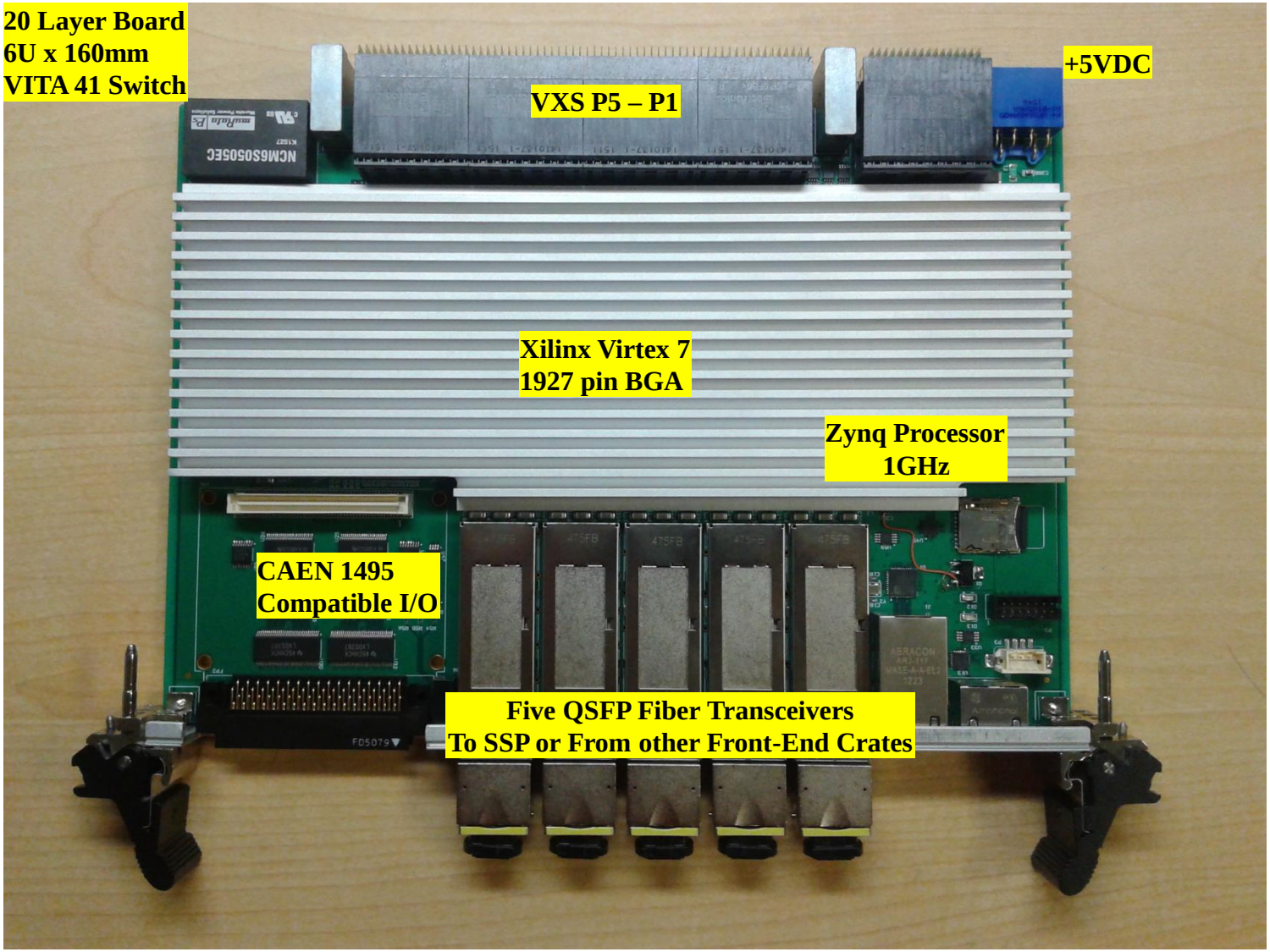


Hall B – VTP
"The Art of Electronics"

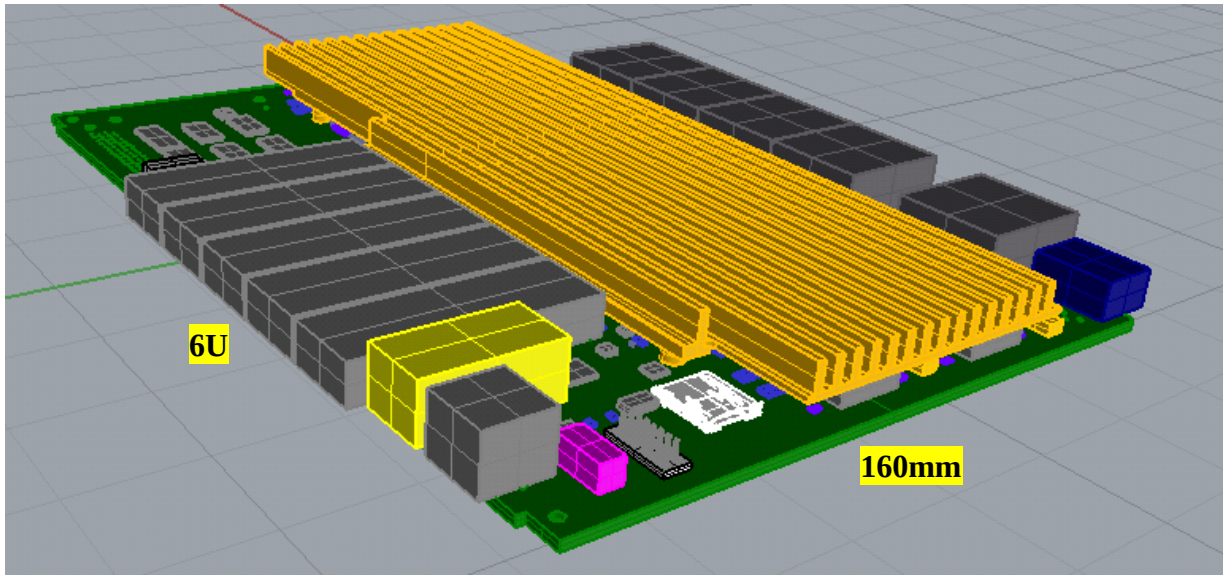
B. Raydo
J. Wilson



Hall B – VTP
"The Art of Electronics Needs Cooling"

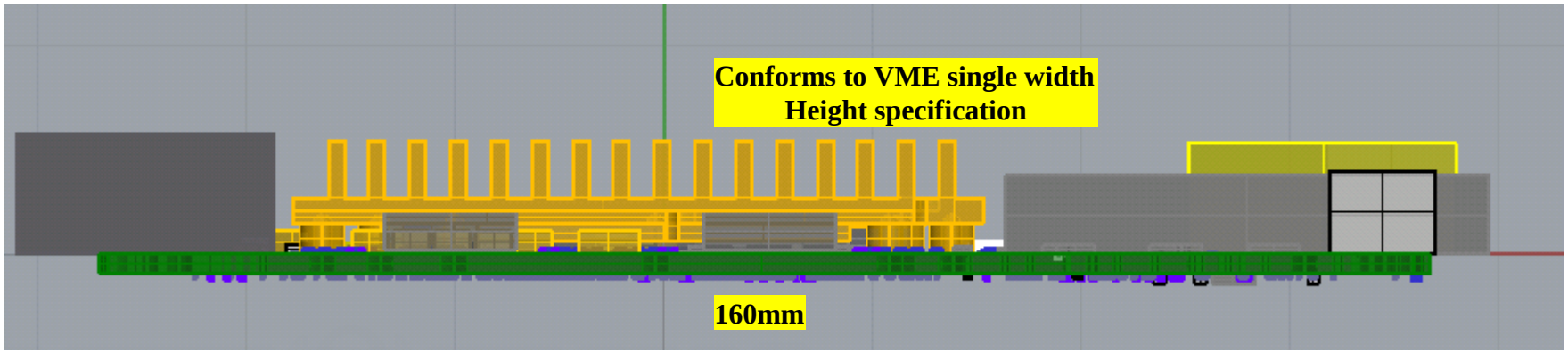


Hall B – VTP
Engineering Issues



VITA41 "VXS" Switch Module

- Only +5VDC available
- Custom Heat sink Design
- Machined Aluminum
  - Contact with Virtex 7, Zynq, and Regulators
- Power dissipation: Up to 40 Watts
- 20 layer board
- 94 mil PCB thickness
- FR408HR Material
- 7263 holes. MIN hole size 8mil
- Full Assembly cost (Qty < 50): ~$7K (USD)
  - Includes:
  - Virtex 7 '550T
  - Heat sink, front panel
  - Solder, Stencil, X-Ray



VTP – VXS Trigger Processor

Ben Raydo
Jeff Wilson
Chris Cuevas

10/40Gb Ethernet

4x QSFP transceivers (up to 34Gbps each)

32x LVDS outputs

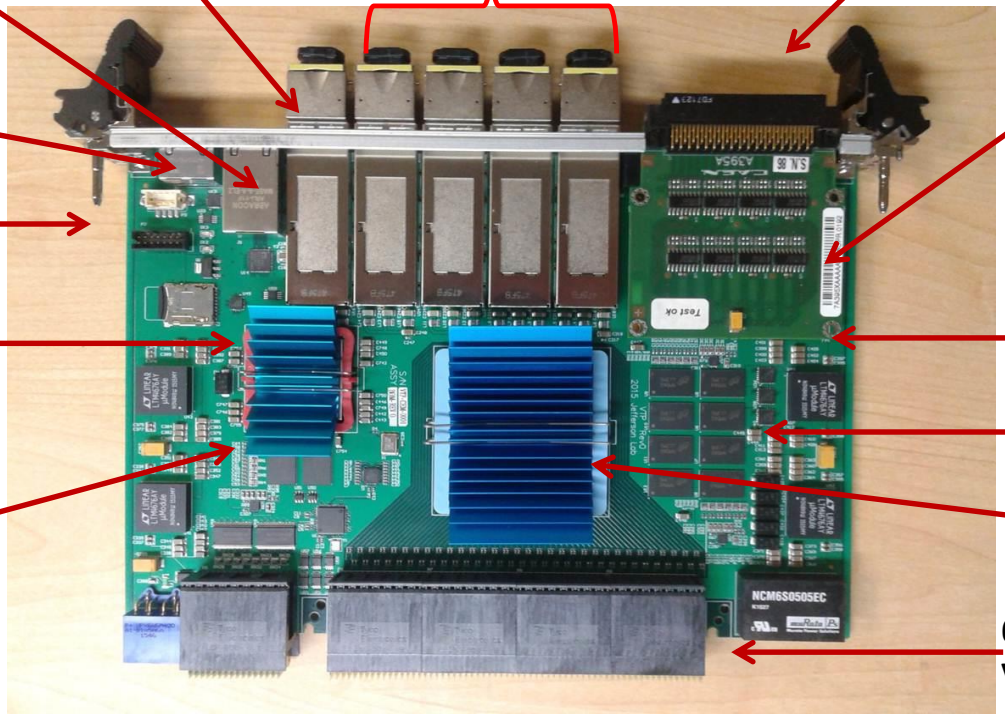
1Gb Ethernet

RS232 Console

SD card O/S & FPGA Storage

1GHz Dual Core ARM Processor [Xilinx Zynq] (Linux OS)

1GByte DDR3 Processor Memory



V1495 compatible expansion Interface:

- 8 ch DAC
- 32 ECL/LVDS outputs
- 32 Anylevel Differential Inputs

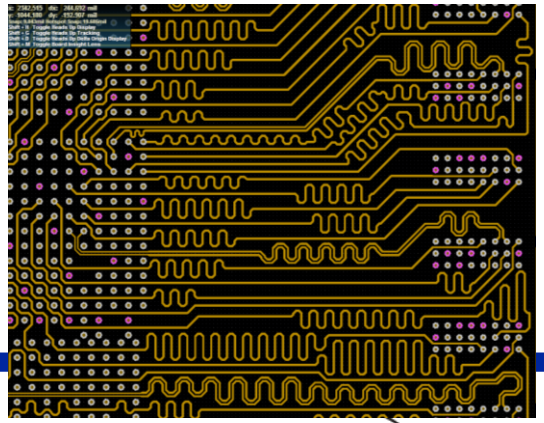
2GB DDR3 #1 (FPGA app specific)

2GB DDR3 #2 (FPGA app specific)

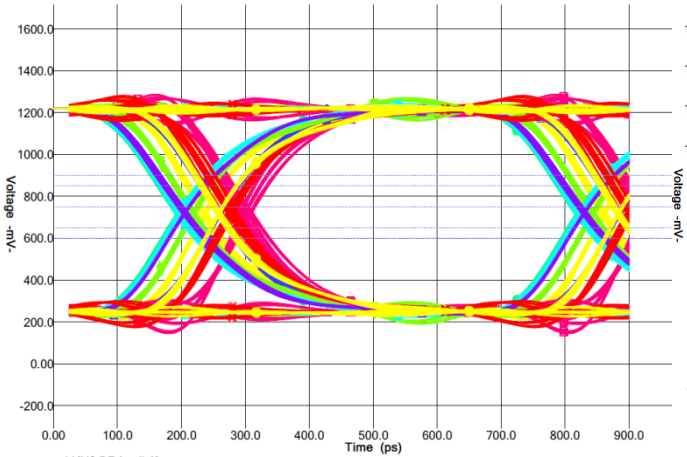
Virtex 7 550T FPGA

64 TX, 64 RX @ up to 8.5Gbps VXS payload interfaces

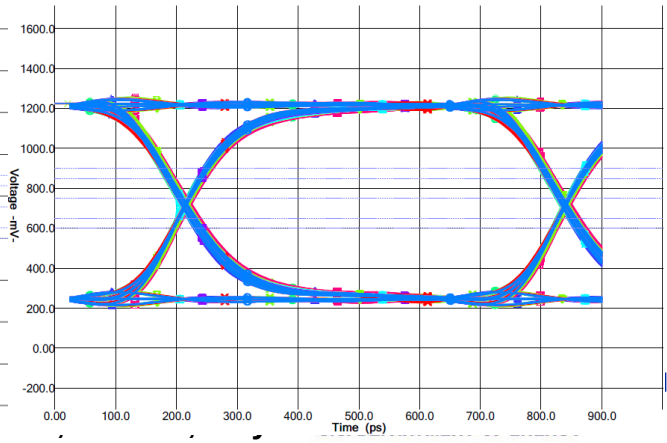
DDR3-1600 Trace/Package Deskewing:



DDR3-1600 byte eye before deskew:

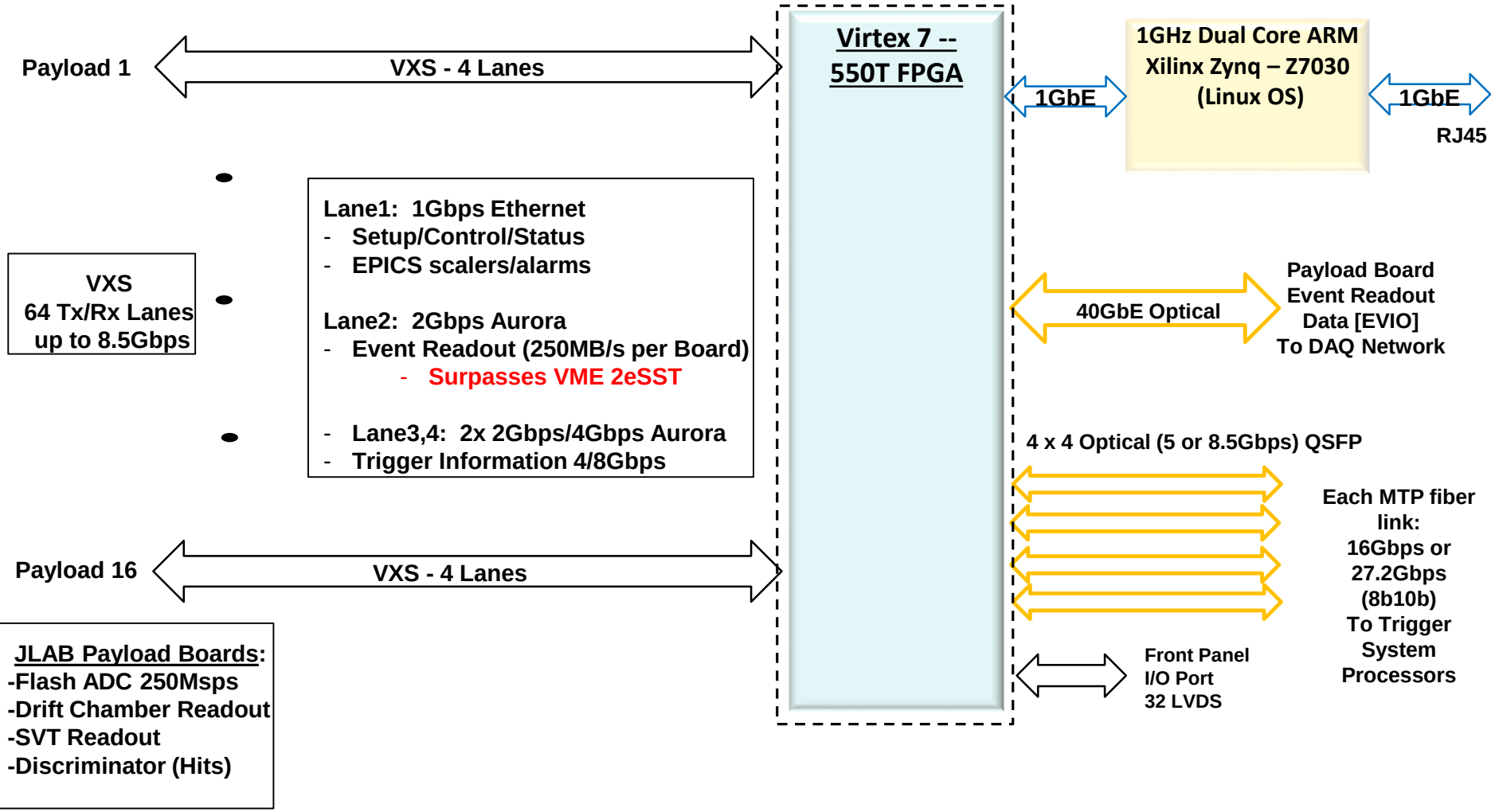


DDR3-1600 byte eye after deskew:



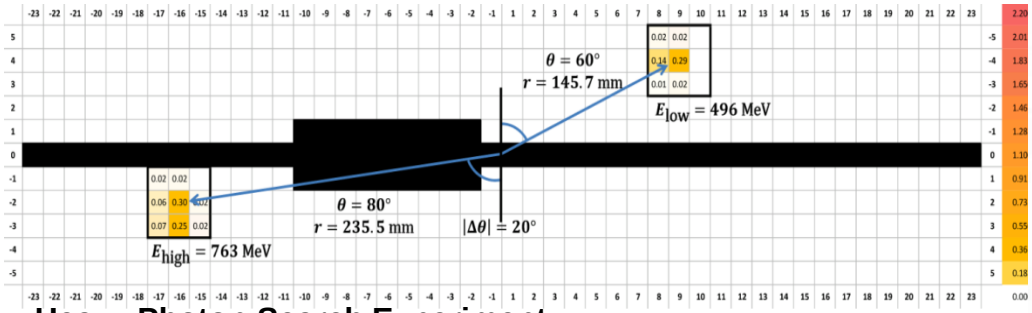
High Speed Serial – The Future
No VME controller – VTP For Control/Readout/Trigger

B. Raydo
J. Wilson
C. Cuevas



VXS TRIGGER PROCESSOR
Complex High Level Trigger Applications

Calorimeter (Cluster Finding):



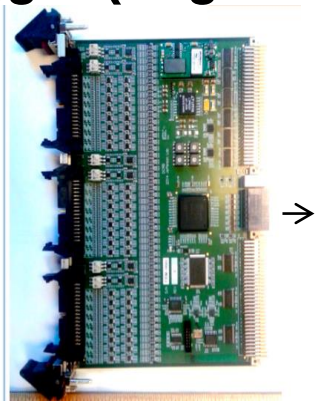
Heavy Photon Search Experiment:

Trigger Cuts:

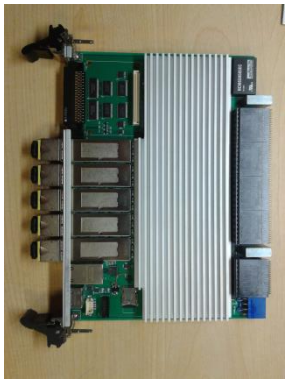
- Energy sum, $E_{min} \leq E_{top} + E_{bottom} \leq E_{max}$
- Pair time coincidence, $|t_{top} - t_{bottom}| \leq \Delta t_{max}$
- Energy difference, $|E_{top} - E_{bottom}| \leq \Delta E_{max}$
- Energy slope, $E_{cluster\_with\_min\_energy} + R_{cluster\_with\_min\_energy} \times F_{energy} \leq Threshold_{slope}$
- Co-planarity, $|tan^{-1}(\frac{X_{top}}{Y_{top}}) - tan^{-1}(\frac{X_{bottom}}{Y_{bottom}})| \leq Coplanarity_{angle}$
- Number of hits in 3x3 window, $\#hits_{3x3} \geq HitThreshold$

Drift Chamber Trigger (Segment/Track Finding):

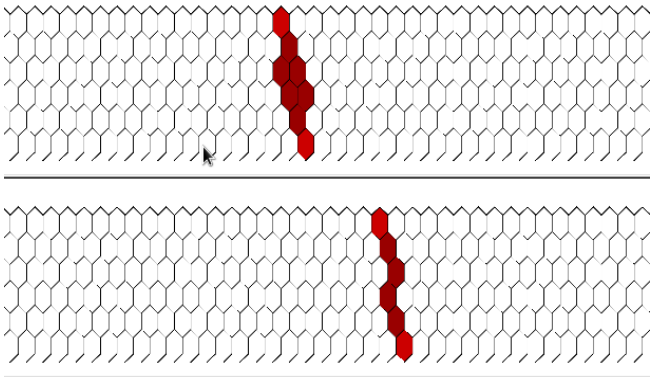
CLAS12 Drift Chamber
(1 sector/1 region shown)
1344 Anode wires



x14 DCRB
96-CH 1ns TDC



VTP



Reports track segment position
and angle to next stage trigger

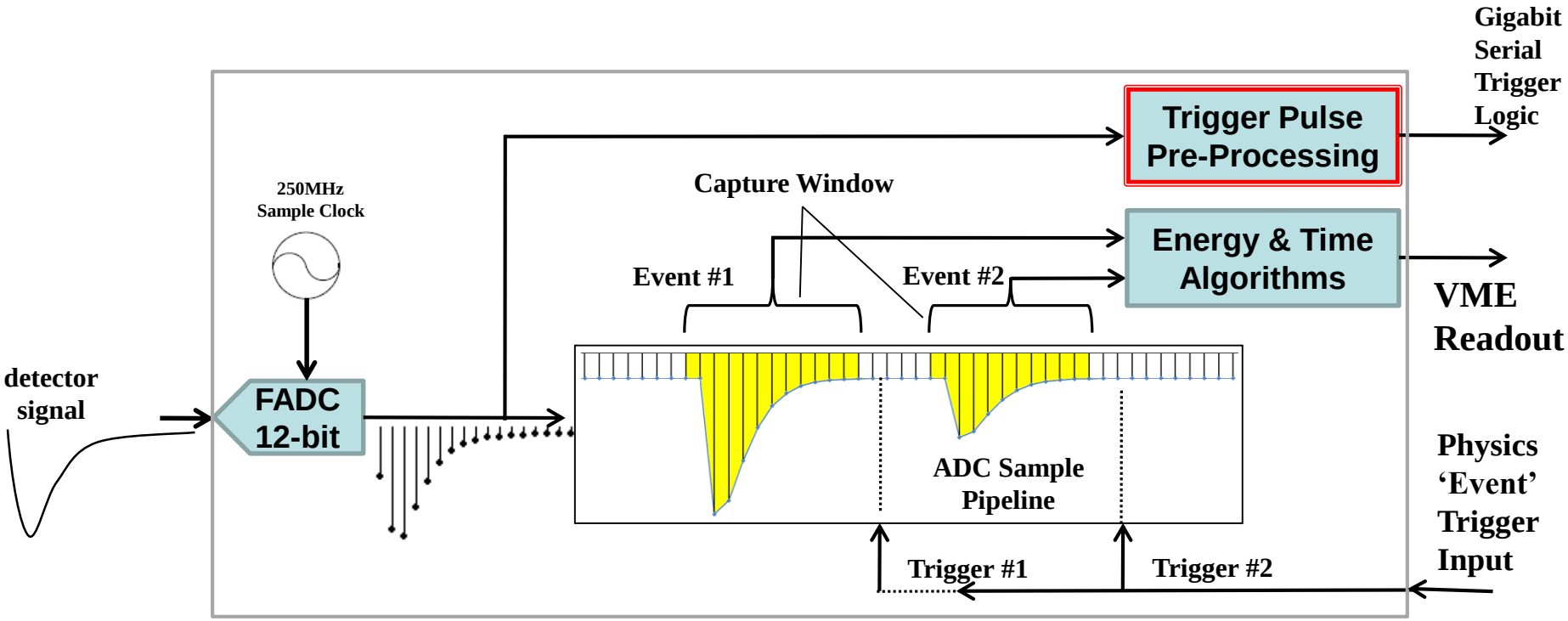
Summary

- VXS solution for 12GeV DAQ and Trigger Electronics has been proven
  - Robust, high reliability serial back-planes, QSFP (optical) transceivers
  - Extremely low failure rate
- VXS offers elegant high speed serial links from each payload slot
  - We use these Gigabit serial links for L1 Trigger Decisions
  - VTP will be used as Event Readout controller
    - Serial connectivity easily surpasses VME 2eSST data rate
    - VTP includes 40GbE port to stream event data
- VTP will support complex high level trigger algorithms at the 'crate' level
  - Process trigger information from multiple crates for large detectors
  - Combine detector sub-systems for Global Trigger
- VTP production boards are scheduled for delivery mid-summer

- Questions?

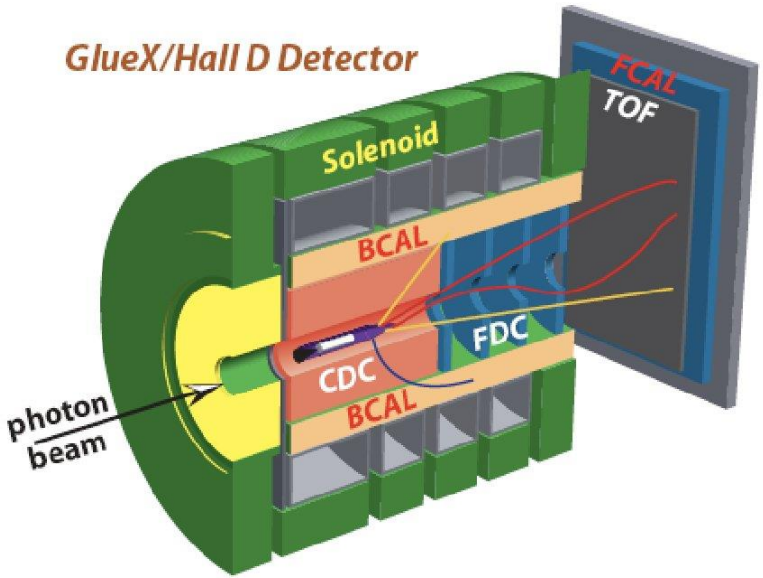
BACK-UP

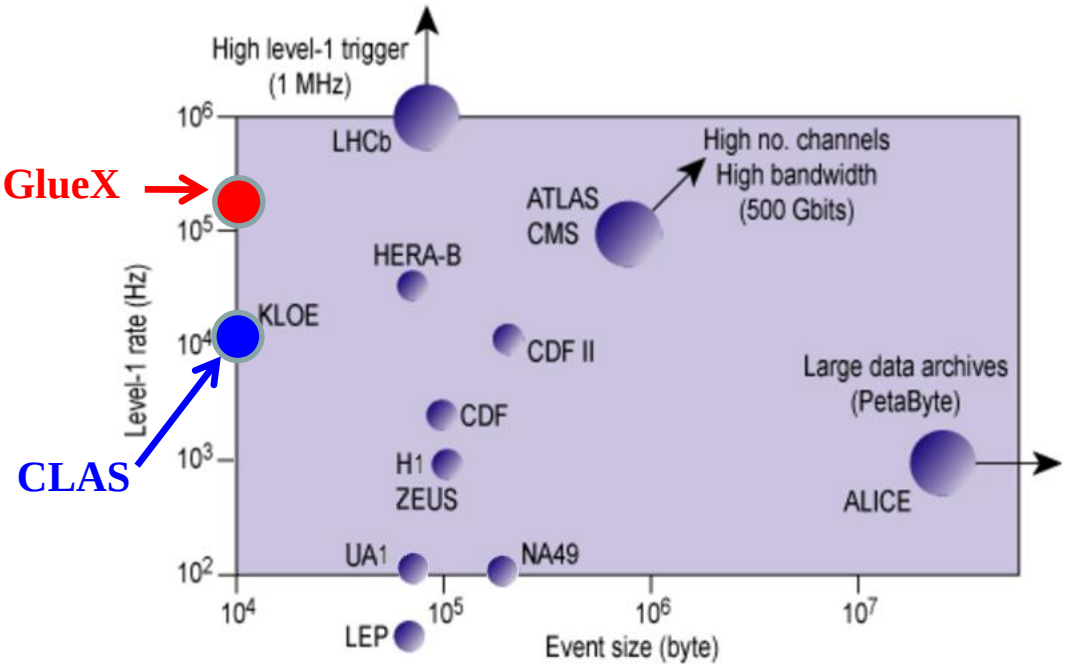
Modern Method of Signal Capture



- 250MHz Flash ADC stores digitized signal in 8μs circular memory.
- Physics "Event" extracts a window of the pipeline data for pulse charge and time algorithms
- Trigger output path contains detailed information useful for cluster finding, energy sum, etc.
- Hardware algorithms provide a huge data reduction by reporting only time & energy estimates for readout instead of raw samples

Comparison to CLAS in Hall B





	Hall D-GlueX	Hall B-CLAS
Channel Count:	~20k	~40k
Event Size:	~15kB	~6kB
L1 Rate:	200kHz	10kHz
L1 Data:	3GB/s	60MB/s
To Disk:	L3, 20kHz, 300MB/s	L2, 10kHz, 60MB/s

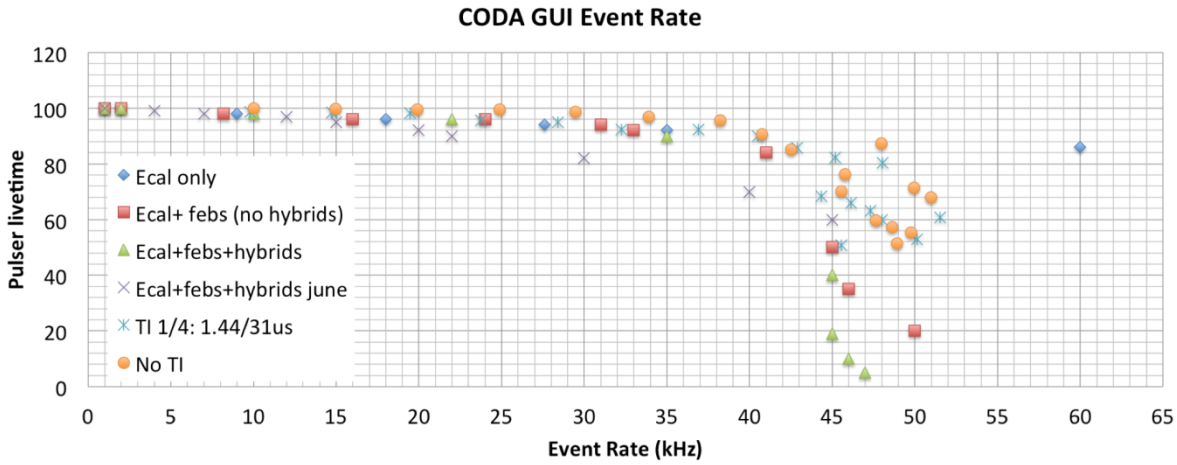
Flash ADC 250MHz

- 16 Channel, 12-bit
  - 4ns continuous sampling
  - Input Ranges: 0.5V, 1.0V, 2.0V (user selectable via jumpers)
  - Bipolar input, Full Offset Adj.
  - Intrinsic resolution – σ = 1.15 LSB.
  - 2eSST VME64x readout
  - Several modes for readout data format
    - Raw data
    - Pulse sum mode (Charge)
    - TDC algorithm for timing on LE
  - Multi-Gigabit serial data transport of trigger information through VXS fabric
  - On board trigger features
    - Channel summing
    - Channel coincidence, Hit counters
  - 2 Pre-production units extensively tested
  - Automatic Test Station is complete
  - Engineering Run – 40 Delivered!
    - 18 Hall D
    - 17 Hall B
    - 685 Boards for all Halls
  - Production Procurement FY12 (>$2M).

DAQ

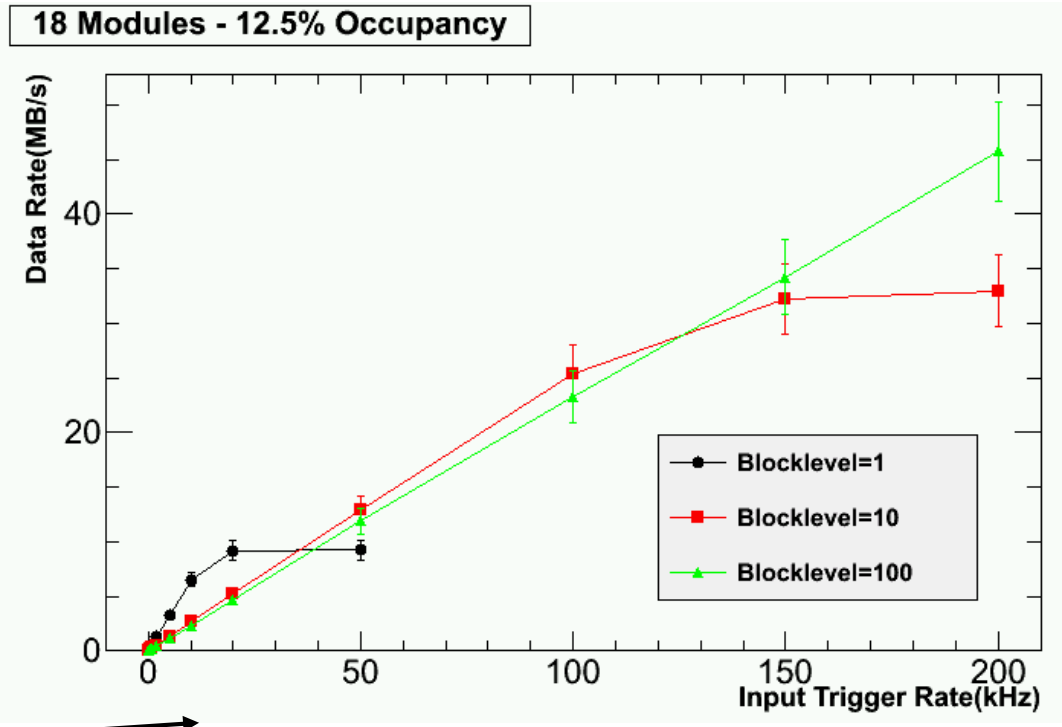
- Forward carriage DAQ electronics installation is almost complete, remaining electronics (VTPs) are ordered and will be installed within few month
- Space Frame and Subway DAQ electronics installation in progress
- Fiber Ethernet and trigger network complete
- Counting room complete
- DAQ software is operational, development continues
- ECAL, PCAL and FTOF detectors are taking data; CTOF, DCRB, SVT, etc. tests

DAQ rate in current HPS run.[45kHz] Expect similar performance for CLAS12 >180MBytes/sec



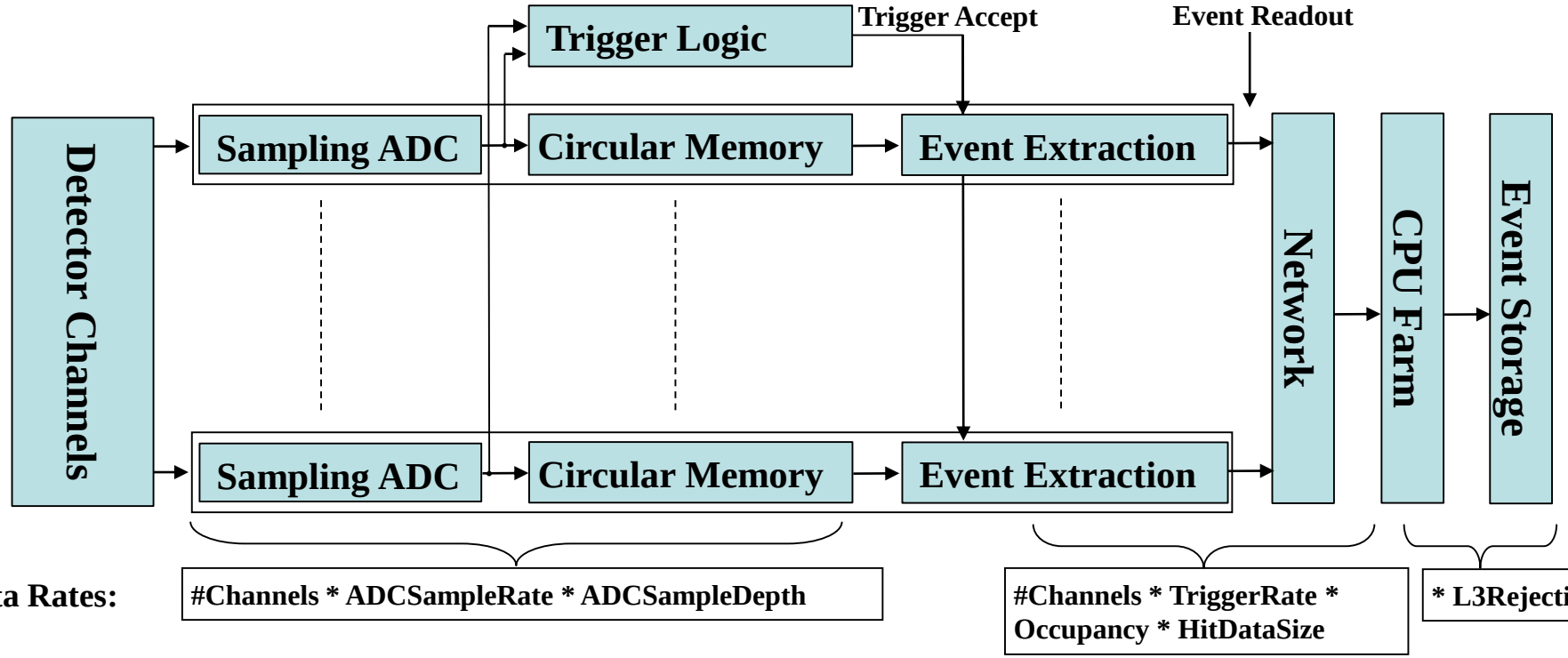
Two DAQ Crate Testing: FY11

- Pre-Production and 1st article boards have been delivered
- Significant effort for circuit board fabrication, assembly and acceptance testing
- System testing includes:
  - Gigabit serial data alignment
    - ✓ 4Gb/s from each slot
    - ✓ 64Gb/s to switch slot
    - ✓ Crate sum to Global crate @8Gb/s
  - Low jitter clock, synchronization
    - ✓ ~1.5ps clock jitter at crate level
    - ✓ 4ns Synchronization
  - Trigger rate testing
  - Readout Data rate testing
  - Bit-Error-Rate testing
    - -Need long term test (24/48 hrs)
  - Overall Trigger Signal Latency
    - ✓ ~2.3us (Without GTP and TS)



200KHz Trigger Rate!

Pipelined DAQ & Trigger Architecture



- All channels are continuously sampled and stored in a short term circular memory

- Channels participating in trigger send samples to trigger logic. When trigger condition is satisfied, a small region of memory is copied from the circular memory and processed to extract critical pulse details such as timing & energy. This essentially makes the event size independent of ADC sampling rate, depth, and number of processed points.

SCOPE OF 12 GeV UPGRADE

Parameter	Present JLab	Upgraded JLab
Number of Halls	3	4
Number of passes Halls A/B/C	5 (for max energy)	5 (for max energy)
Max Energy to Halls A/B/C	up to ~6 GeV	up to ~11 GeV
Number of passes to Hall D	New Hall	5.5
Energy to Hall D	New Hall	12 GeV
Current – Hall A & C	max ~180 μA combined	max ~85 μA combined (higher at lower energy)
Current – Hall B & D	(B) Up to 5 μA max	(B, D) Up to ~5 μA max each
Central Helium Liquefier (CHL)	4.5 kW	9 kW
# of cryomodules in LINACS	40	50
Accelerator energy per pass	1.2 GeV	2.2 GeV

Routinely provide beam polarization of ~85% now, same in 12 GeV era

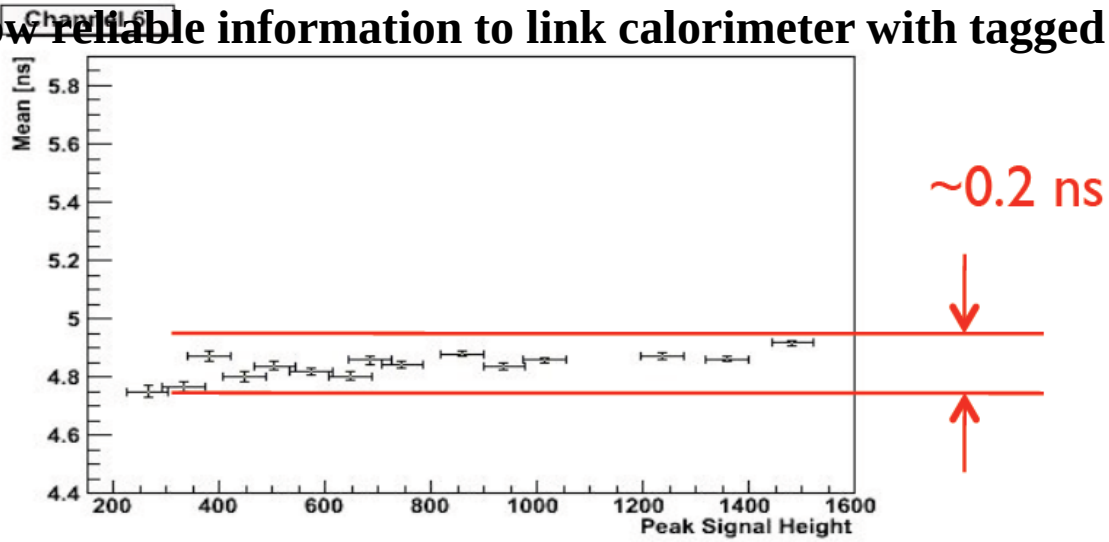
3.5 FADC Sampling – Timing Accuracy

Hall D FCAL PMT: FEU 84-3

- Timing algorithm developed & tested by Indiana University for the Hall D forward calorimeter.

- Implemented on the JLab FADC250 hardware achieving <300ps timing resolution on 50% pulse crossing time with varied signal heights.

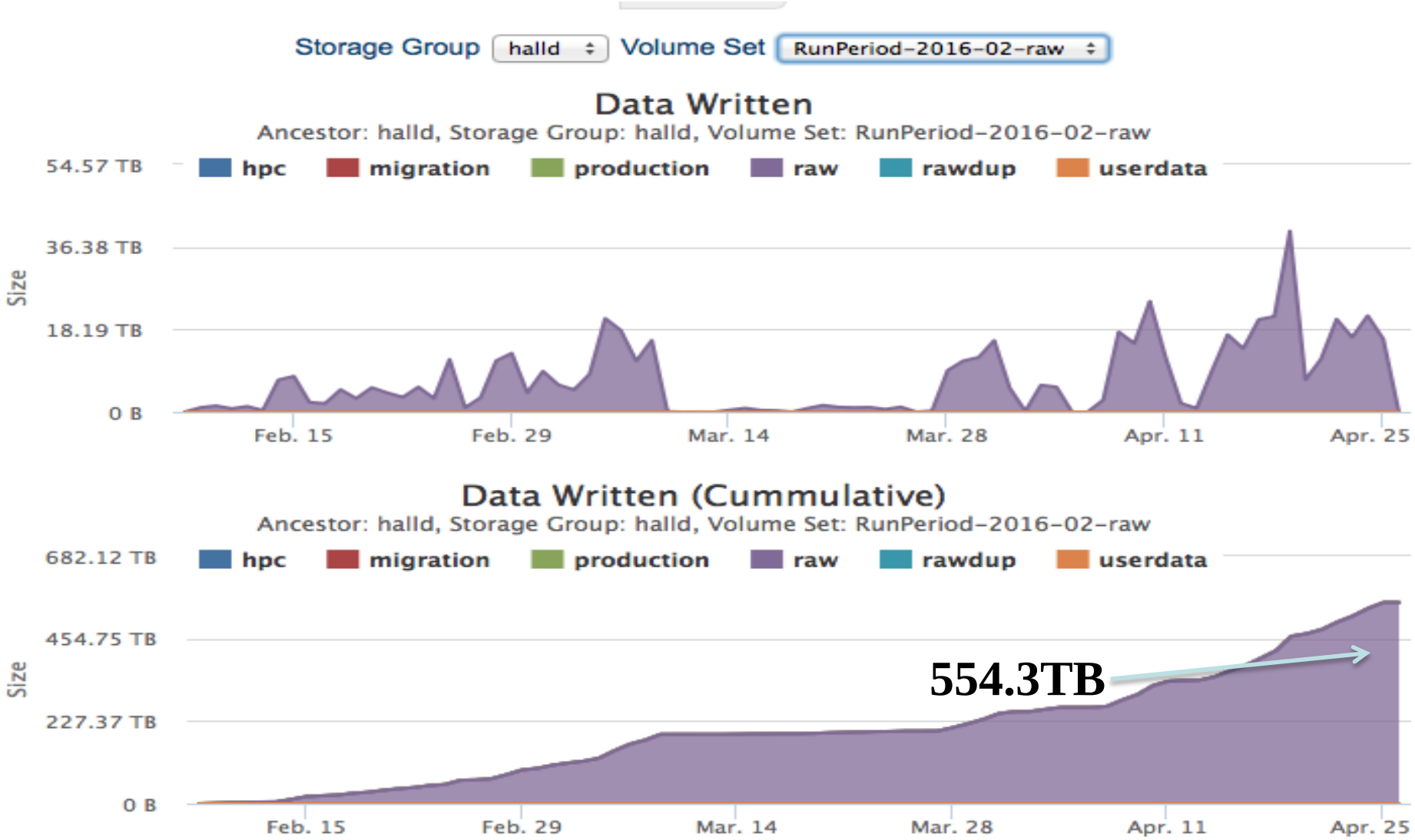
- Resolution allow reliable information to link calorimeter with tagged electron bunch.



Typical timing resolution achieved ~1/10 the sample rate. The PMT shape will drive the ADC sample rate & depth requirements.

From: GlueX Doc# 1258-v1

GlueX Data Volume



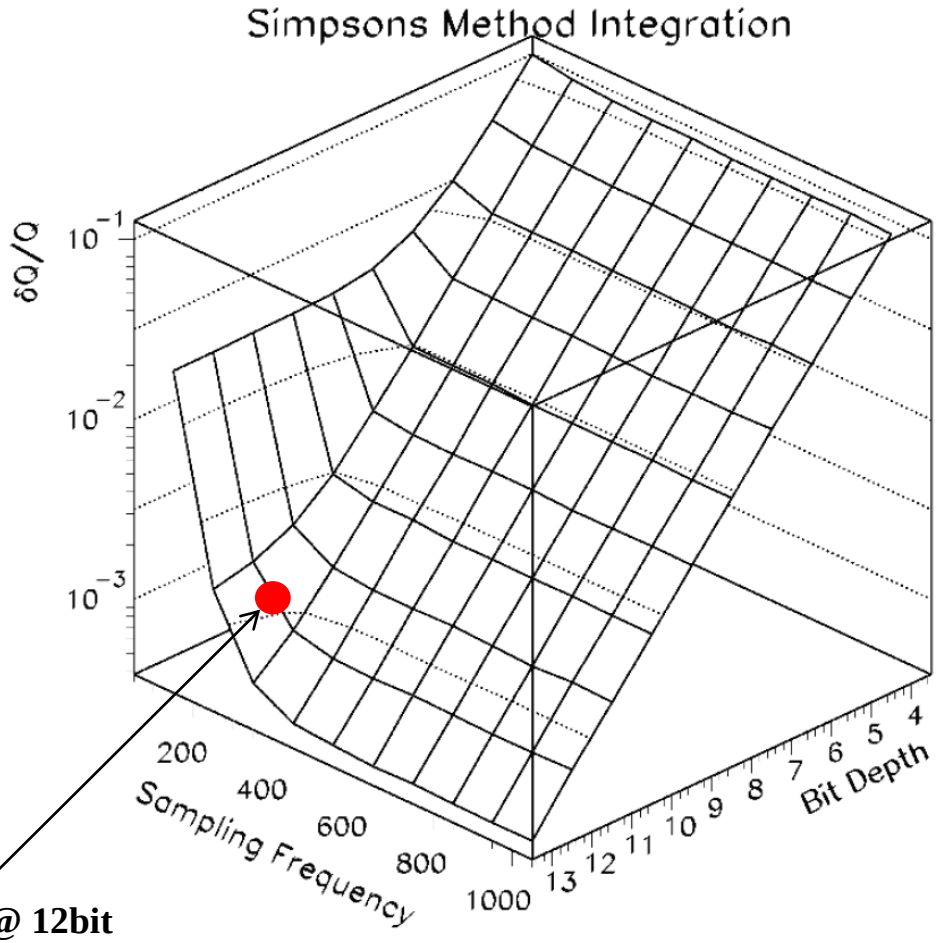
3.4 FADC Sampling – Charge Accuracy

Hall D FCAL PMT: FEU 84-3

-10,000 Random height pulses 10-90% full scale of ADC range simulated

- Sampling frequency makes little difference beyond 250MHz at 12bit, providing ~0.1% charge resolution

- PMT pulse shape dominates sample frequency and bit depth of ADC



250MHz @ 12bit