Low Phase Noise Local Oscillator and Clock Generation for Cavity Field Detection

Mateusz Żukociński, Krzysztof Czuba, Matthias Hoffmann, Frank Ludwig, Uros Mavrič, Łukasz Zembala

***Abstract*– The paper presents local oscillator (LO) and clock (CLK) generation module of ultra-low phase noise level. The LO signal is used in superheterodyne receiver of Low-Level RF (LLRF) field detector. The CLK signal is used as a low jitter sampling clock for analog-to-digital converters (ADC) of the LLRF digitizer. These high performance signals allow precise control of electromagnetic field in superconducting RF cavities that accelerate electrons in the new generation of Free-Electron Laser (FEL) machines. Both LO and CLK signals are generated in a single module based on PCB circuit. The module meets stringent electrical and mechanical requirements of the accelerator system. The paper discusses a few most promising scenarios of the signal generation. Design considerations, modelling issues, circuit prototypes and final realization of the module are described. Phase noise measurements proof excellent results achieved. The designed module produces up to 0.5 W of low phase noise 1354 MHz signal of single femtoseconds of integrated RMS time jitter, noise floor of -165 dBc/Hz and spurious-free range better than 90 dBc.**

I. Introduction

When designing electron accelerator control system (LLRF system, acronym for Low-Level RF) for the new generation of Free-Electron Laser (FEL) machines there are many considerations. First is superior performance focused on ultra-low phase noise which contributes to the quality of the cavity electromagnetic field in superconducting modules, stability of accelerated electron bunches arrival time and finally to the output laser light of FEL [1]. Other important goals for the system are drift minimization, remote control and diagnostics, high reliability and compact form factor. One of the crucial subsystems is Local Oscillator (LO) generation and Clock (CLK) generation. The RF cavity probe signal of frequency 1300 MHz is mixed with LO signal 1354 MHz and downconverted to an intermediate frequency (IF) of 54 MHz. This lower frequency IF signal holds the original amplitude and phase information of the field inside the cavity. The IF signal is sampled by analog-to-digital converter (ADC) with 81 MHz CLK and processed by digital part of the LLRF (Fig. 1). Accuracy of the cavity field detection critically influences regulation of the accelerating field. That is why phase noise performance of the signal is of our interest here. This is even more critical when vector sum of probe signals from multiple cavities is calculated and used for field regulation [1].

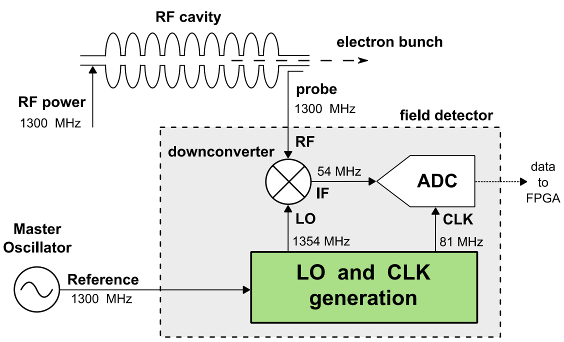

Fig. 1 Diagram of RF cavity field detection

During our research different LO generation scenarios have been considered and tested. Performance and small form factor for PCB integration were of our interest. Phase-Lock Loop (PLL) based technique and mixing technique were considered to be the most promising. Technology limits where performance and the size of VCO's and filters are in trade-off have been met. Detailed discussion on PLL-based LO generation and its prototype realization has been already presented in [2]. Performance of small PCB-mount VCOs building PLL circuits is still not satisfactory for demanding accelerator application. In this article we have focused on mixing technique for LO generation which gives better performance vs. circuit size (integration). Several scenarios are possible but only two the most promising are presented. Critical design considerations were recognized and are discussed below.

Modelling of phase noise allows predicting circuit performance but in most cases data required are not available which makes it necessary to perform measurements of each individual component. Here, single-sideband phase noise characteristics ***L****(f)* [3] were captured what allowed calculating integrated RMS phase and time jitter values [3]. In our research residual phase noise of different LO generation circuits and their components were found using 2 DUT phase detector test methodology [3,4]. Exemplary results will be discussed later in this paper.

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M. Żukociński, K. Czuba and Ł. Zembala are with the Warsaw University of Technology, Nowowiejska 15/19, 00-665 Warsaw, Poland (telephone: +48 234 7876, e-mail: M.Zukocinski@elka.pw.edu.pl).

M. Hoffmann, F. Ludwig and U. Mavrič are with the department of the beam control of Deutsches Elektronen-Synchrotron (DESY), Notkestrasse 85, D-22607 Hamburg, Germany.

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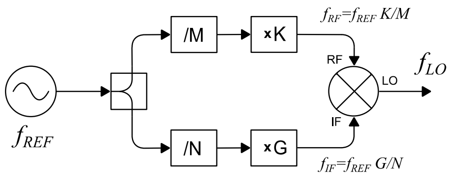
II. Mixing Technique

Passive double-balanced mixers are known as low noise frequency converting devices [4,5]. This is widely used in RF systems, e.g. in superheterodyne (non-zero IF) receivers [4,6]. Thanks to specific properties of the mixers and their low noise behaviour they find application as phase detectors as well [5]. This is used in measurement technology and PLL techniques. Here, mixer as a frequency converter is used to generate LO signal.



$$f_{LO} = f_{RF} \pm f_{IF}$$

$$f_{LO} = f_{REF}\left(\frac{K}{M} \pm \frac{G}{N}\right)$$

Fig. 2 General scheme of signal synthesis using mixer

There are various architectures of signal conversion based on mixing (heterodyning). In general the LO signal is synthesized by mixing of two frequencies which sum or difference produces signal of desired LO frequency (Fig. 2).

To preserve phase coherence of signals in the accelerator system a common reference signal (REF) is used. Then the RF (heterodyne) and IF (intermediate frequency) signals can be synthesized from the REF using, in general, combination of frequency dividers and frequency multipliers (Fig. 2).

After system analysis the IF frequency of 54 MHz (precisely 1300 MHz divided by 24 = 54.16(6) MHz) was chosen. Consecutively the LO signal has frequency of 1354 MHz. Then two LO generation schemes were selected for further prototyping and testing. First one is a single-stage mixing circuit presented in Fig. 3.

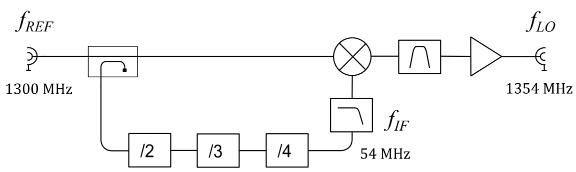


Fig. 3 Diagram of single-stage mixing LO generation

III. Phase Noise Analysis

Total phase noise added by the circuit from Fig. 3 can be modelled with help of noise theory [7]. Below a noise model of single-stage mixing LO generation circuit from Fig. 4 is analyzed. Parameters *Δφ* represent RMS phase jitter integrated in certain band of interest (here 10Hz – 1MHz).

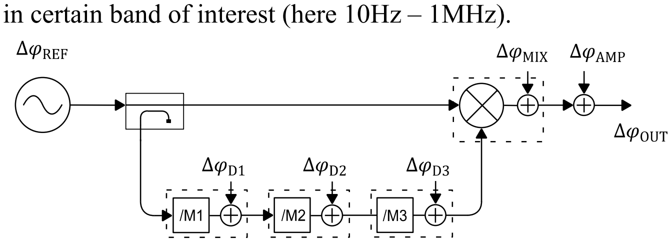


Fig. 4 Model of single-stage mixing circuit for jitter calculations.

According to Fig. 4 the output RMS phase jitter equals:

$$|\Delta\varphi_{out}|^2 = \left[\left[\frac{|\Delta\varphi_{REF}|^2}{{M_1}^2} + |\Delta\varphi_{D1}|^2\right]\cdot\frac{1}{{M_2}^2} + |\Delta\varphi_{D2}|^2\right]\cdot\frac{1}{{M_3}^2} + |\Delta\varphi_{D3}|^2 + |\Delta\varphi_{MIX}|^2 + |\Delta\varphi_{AMP}|^2 \quad (1)$$

The residual RMS phase jitter of the circuit is then:

$$|\Delta\varphi_{res}|^2 = \left[\frac{|\Delta\varphi_{D1}|^2}{{M_2}^2} + |\Delta\varphi_{D2}|^2\right]\cdot\frac{1}{{M_3}^2} + |\Delta\varphi_{D3}|^2 + |\Delta\varphi_{MIX}|^2 + |\Delta\varphi_{AMP}|^2 \quad (2)$$

IV. Realization

The LO and CLK generation module was realized as a PCB circuit enclosed in an aluminium case (Fig. 5). Apart of the main functionality which is the LO generation the module is responsible for synthesis of low-jitter 81 MHz clock signal (CLK) which is used for ADCs in digitizer module of the accelerator RF cavity signal receiver (Fig. 1). This makes the module responsible for generating the most crucial signals from the low-noise receiver point of view (LO and CLK). The clock signal is synthesized by frequency divider circuit optimized for low-noise. An important feature of this circuit is reset functionality which is needed to force or re-establish synchronism between CLK signals, and thus ADCs, in different parts of the accelerator system.

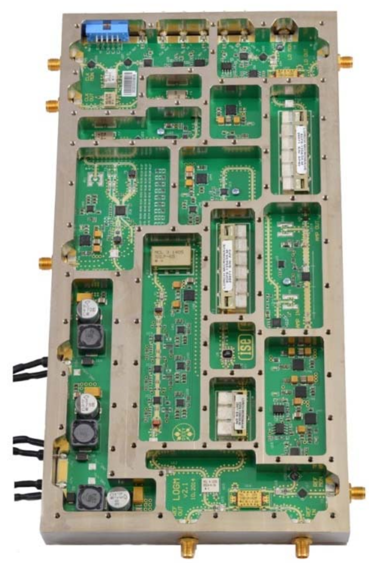


Fig. 5 Photography of LO generation module (open lid)

V. Results

Measured performance of the single-stage mixing 1354 MHz LO generation module meets specification for FEL accelerator control system. Absolute phase noise characteristics in Fig. 5 show phase noise floor of -165 dBc/Hz and no unexpected spurs. The 2 DUT tests allowed to measure residual phase noise of the module (Fig. 6). Based on that the RMS time jitter integrated in band 1 MHz ÷ 10 Hz was estimated to be 2 fs (phase jitter of 1 mdeg). RMS time jitter of the measurement setup itself was 0.5 fs (0.2 mdeg).

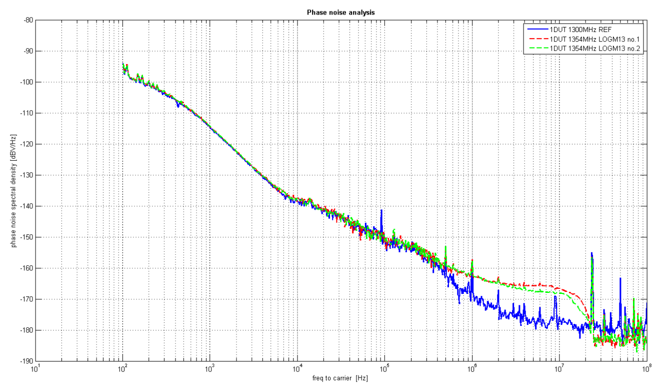


Fig. 6 Absolute phase noise characteristics of LO generation module from Fig. 5

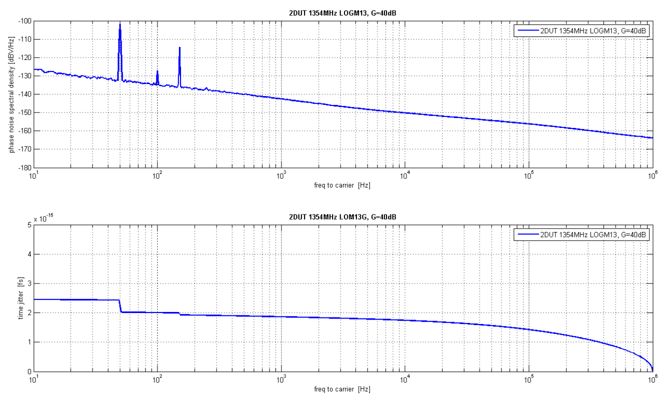


Fig. 7 Residual phase noise characteristic (top) and cumulative time jitter (bottom) for module from Fig. 5

VI. Summary

Ultra-low phase noise LO and CLK generation module based on single-stage mixing technique was successfully designed. This module finds application in FEL accelerators instrumentation. Results down to single femtoseconds of the LO residual RMS time jitter integrated in 10Hz ÷ 1 MHz band was achieved. As a result of our research a family of ultra-low phase noise LO and CLK generation modules was developed. In [9] a module designed for MicroTCA.4 industry standard [10] was presented. A family of universal LO generation modules that operate with frequencies from hundreds of MHz up to 6 GHz is under development.

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