Concentrator for the Readout of the PANDA Micro Vertex Detector based on MicroTCA

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***Abstract*– The Micro Vertex Detector (MVD) will be used as the central tracking detector in the PANDA (AntiProton Annihilation at Darmstadt) detector system which is under development for the future accelerator facility FAIR in Darmstadt, Germany. The design of the MVD is based on silicon strip detectors at the outer layer and on silicon pixel detectors at the inner layers. Data from the readout ASICs in the front end will be sent via GBT optical links to a multiplexing layer aggregating them to 10 Gbit/s optical uplinks to the Level-1 Trigger network. The multiplexing layer will be based on MTCA.4 using the HGF-AMC, a versatile MTCA.4 module developed by DESY in cooperation with KIT. In order to extend the multiplexing capabilities of the HGF-AMC, a Rear Transition Module (RTM) with 8 optical links has been designed.**

I. Introduction

The PANDA (Anti**P**roton **An**nihilation at **Da**rmstadt) detector system is a multipurpose fixed target experiment foreseen for the future accelerator facility FAIR in Darmstadt and will be located at the High Energy Storage Ring (HESR) [1]. The physics program of PANDA will address open issues in strong QCD, e.g. precision charmonium spectroscopy, glueballs and hybrids. In the target spectrometer of PANDA a micro-vertex detector (MVD) will be used as the central tracking detector for charged particles. The MVD is the innermost tracking detector for charged particles. The design of the MVD is based on pixel and microstrip silicon sensors. Currently, INFN Torino is developing ToPIX, a front-end ASIC for the readout of the pixel sensors [2]. Off-detector transfer of the TOPIX data is accomplished with the radiation-tolerant GBT chipset, which is under development at CERN. The GBT implements a serial optical link at a nominal data rate of 3.36 Gbit/s [3]. ZEA-2, the central electronics facility of Forschungszentrum Jülich, contributes to the development of the readout electronics for the MVD.

II. PANDA Data Acquisition and MicroTCA

The planned PANDA DAQ will be designed for a free-running triggerless operation. Front-end electronics at each detector channel are responsible for a continuous digitization of the physical signals, without any trigger hardware. Via serial channels, the digitized data are sent to front-end concentrator/multiplexer modules, which combine several detector channels and send the combined data via serial optical links to the so-called Level 1 Network. The Level 1 Network consists of interconnected ATCA crates, containing so-called compute-node modules. On the compute-nodes feature extraction algorithms are implemented in order to reduce the detector data. From the Level 1 Network the reduced data are sent to the so-called Event Selection Network, where a computer farm is responsible for event building and transfer to mass storage.

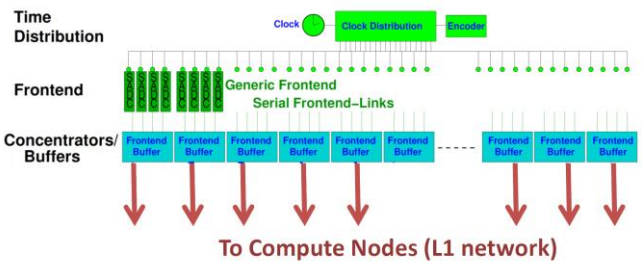

Fig. 1: Front-end architecture of the PANDA DAQ system [1]

The hardware platform for the concentrator/multiplexer modules depends on the requirements of the detector frontend electronics. In many cases MicroTCA [4][5][6] is a reasonable choice. For the MVD is has been decided to use MTCA.4 [7], which has become very popular in the physics community during the recent years, at the concentrator/buffer layer. Each MTCA.4 module will receive 3 GBT-Links and translate them to a 10 Gbit/s uplink to the compute-nodes, as shown in Fig. 2. Clock and timing information is decoded from the timing system SODA and distributed via the dedicated clock and trigger lines on the backplane, which have been defined by MTCA.4. MicroTCA provides a standard module and crate management and allows the addition of a dedicated local CPU in the crate for the implementation of slow control functions.

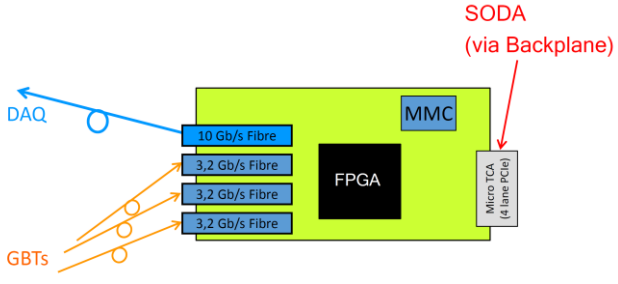

Fig. 2: Functionality of the MVD multiplexing module (MMB)

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III. The HGF-AMC

For the implementation of the multiplexing modules a variety of candidates are available, which have been developed by different research institutions. For the MVD the so-called HGF-AMC, a powerful MTCA.4 module shown in Fig. 3 that was developed by DESY together with KIT, has been selected.

Fig. 3: Photo of the HGF-AMC

Core of the HGF-AMC is a Xilinx Kintex7 FPGA (XC7K325TFFG900). A 64 bit wide interface to a 4 GBytes DDR3 SODIMM module has been implemented that supports 1600 MT/s. It is equipped with a FMC interface (LPC connector) and a µRTM-Interface. The AMC interface supports PCIe (4 GTX lanes) and GB-Ethernet (1 GTX lane) to the MCH. Additionally, 4 GTX lanes are used for point-to-point direct connections to different AMCs. 1 GTX lane is routed to the FMC interface and 2 GTX lanes are routed to the µRTM-interface, in addition to 46 LVDS lanes at this interface. For the implementation of a high speed external optical interface (4 x 12.5 Gb/s) 4 GTX lanes are routed to 4 SFP+ modules on the front-panel. The IPMI–compliant Module Management Controller is based on an Atxmega128A1. The SFP+ ports on the front panel allow a straight forward implementation of the aggregation of 3 GBT links to one 10 GB/s uplink.

IV. Optical Link Rear Transition Module

In order to increase the multiplexing level of the HGF-AMC it was decided to design an 8 port optical link Rear Transition Module (RTM) for the HGF-AMC shown in Fig. 4.

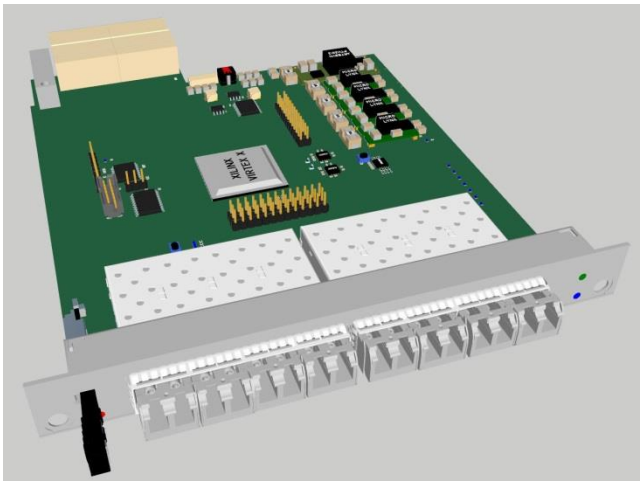

Fig. 4: Optical link RTM for the HGF-AMC

According to the block diagram in Fig. 5 the RTM is equipped with a low cost Artix7 FPGA from Xilinx (XC7A200T). 6 of its GTP transceivers are connected directly to SFP+ modules on the rear panel. Via a multiplexer the remaining to SFP+ modules can be either connected to GTP transceivers of the Artix7 or the GTX transceivers of the Kintex7 on the HGF-AMC, which is the standard configuration for the readout of the MVD. The LVDS lanes on the µRTM-interface support 600 Mb/s. They are grouped in 6 6 bit wide unidirectional ports for the upstream data transfer from the SFP+ modules connected to the GBTs in the fronted, providing sufficient bandwidth for the 3.36 Gb/s data rate. All downstream data transfer to the GBTs is multiplexed over one LVDS lane. In combination with the RTM the HGF AMC can multiplex 9 GBT links to 3 10 Gb/s uplinks to the compute-nodes.

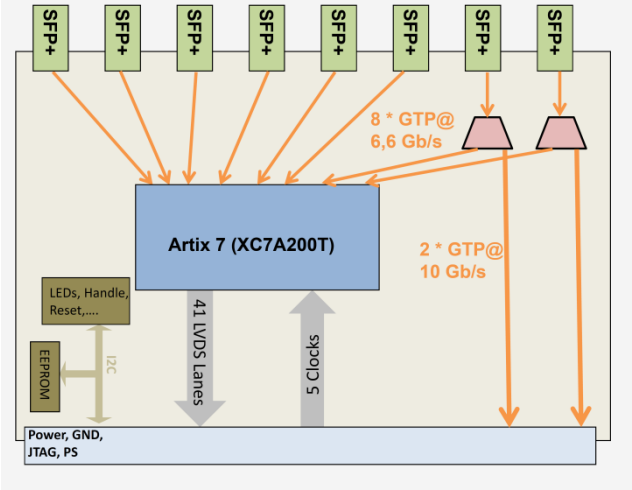

Fig. 5: Block diagram of the optical link RTM for the HGF-AMC

V. FPGA Firmware Architecture

Since the communication protocol to the compute nodes is not standardized yet, it was decided to implement UDP on the uplinks to the Compute Node. This will allow easy

implementation of test systems with readout PCs instead of compute-nodes.

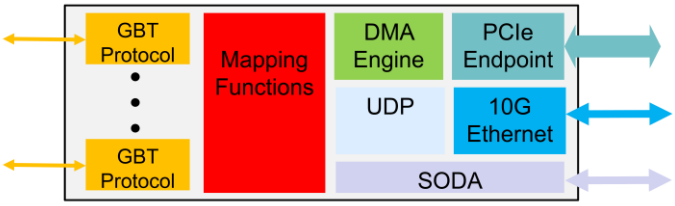

Fig. 6: Function blocks of the FPGA Firmware on the Kintex7

The firmware of the Kintex7 is responsible for the implementation of the GBT protocol based on VHDL source code available from CERN. Central function is the mapping of the GBT communication to the UDP for the uplinks. Timing information and clock form the SODA has to be provided to the GBTs. For slow control information and for smaller lab systems a PCIe endpoint is supported in order to communicate with a local CPU in the MicroTCA crate. It is intended to use the DMA engine from Northwest Logic in combination with the PCIe endpoint.

VI. Status and Future Developments

For development work and lab tests at Forschungszentrum Jülich KIT has produced 4 HGF-AMCs. The design of the optical link RTM has been finished and it is under production, now. First tests for the implementation of the SODA protocol on a Kintex7 have been done which showed that the required locking of the GTX transceiver works properly. The implementation of the Artix7 and Kintex7 firmware is planned for the next year.

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