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The data acquisition system of the DSSD detector for SIRIUS

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We report on the design and performances of the front end electronics and data acquisition system for the double-sided silicon strip detector (DSSD) of the SIRIUS array, to be installed at the focal plane of the S3 spectrometer for SPIRAL 2 at GANIL in 2017. The DSSD placed across the particle path is used to detect the time and position of the implanted heavy ion along with the subsequent energy deposited by the ion alpha decay (several microseconds up to hours later). While the requirement on the energy resolution for the former particles is 5MeV with a range of 500MeV, the alpha particles having a maximum energy of 10MeV need to be measured with a resolution better than 25keV. The dual channel Floating point Charge sensitive amplifier (FPCSA) ASIC, designed to meet these combined requirements, implements an automatic gain switching feature based on its output voltage. Gain switching from high to low gain occurs when the output voltage rises above a configured threshold. The FPCSA returns to high gain 2.5 microseconds later insuring system readiness for alpha detections in the same Si strip.

The complete whole detection and data acquisition chain is currently being integrated at IRFU for full characterization and evaluation of performances. The front end electronic boards for the preamplification of 256 channels were designed at IRFU. The slow control is provided through an I2C link driven by a Raspberry Pi commercial board. The signals are propagated to the back end using 64 HDMI cable assemblies chosen for their high noise immunity and good signal integrity hence allowing improved timing measurements.
The back end electronics and DAQ software are based on GANIL developments, which were adapted to the specific needs and requirements of the DSSD detector and the FPCSA. The 16 Numexo2 boards carry 16 ADC channels to digitize the input signals over 14bits at 200MHz. Each Numexo2 provides access to two Xilinx FPGAs (Virtex5 and Virtex6). A dedicated self-triggering and data concentration firmware was implemented in the Virtex 6 to manage the incoming data flow. A TDC with nanosecond precision (in the experiment's distributed clock domain) will be implemented using available IOSERDES and programmable logic resources for resynchronization purposes. An Ethernet 1000BASE-X link will be used for all communications between the DAQ software and the Numexo2 board through the communication stack of the embedded Linux running on the PPC (inside the Virtex 5). Specific interfaces for slow control and data transfer will soon be available to test the full data acquisition chain. Finally, the DAQ software will implement online data processing algorithms to extract physically meaningful information from the acquired pulses, taking into account the specific shaping induced by the FPCSA.

Preliminary results obtained with the final FE boards and a 14 bit commercial digitizer demonstrate the good performance of the FPCSA. The spectrum of a 3-peak alphas source, measured with this test setup, shows an energy resolution within specifications. System performance at higher trigger rates are expected mid 2016.

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