Digital SPAD Scintillation Detector Simulation Flow to Evaluate and Minimize Real-Time Requirements

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***Abstract*—Radiation detection used in positron emission tomography (PET) exploit the timing information to remove background noise and refine the position measurement through time-of-flight (TOF) information. In PET, very fine time resolution (in the order of 10 ps FWHM) would not only improve contrast in the image, but would also enable real-time image reconstruction without iterative or back-projected algorithms. The current performance limitations will be pushed off through the optimization of faster light emission mechanisms (prompts photons), after which the burden of timing resolution will fall to the readout optoelectronics. Digital SPAD arrays offer compelling possibilities to minimize timing jitter in these future detector systems such per-cell timestamps granularity and per-cell configuration parameters, providing a highly flexible signal processing environment. However, processing hundreds of timestamps per detection event places a toll on the real-time processing, which increases rapidly with embedded channel count. Furthermore, if the processing is sent to an external device such as an FPGA, the bandwidth and related power requirements also increase.**

The simulation flow presented here offers perspectives on how many time to digital converters (TDC) would be required to reach the 10 ps FWHM CTR range for PET. Using this information, designers can estimate the compromises between timing performance, bandwidth requirements, data transmission, power consumption and real-time dataflow processing in the DAQ at the chip and system level. With a standard 1.1 $\times$ 1.1 $\times$ 3.0 mm^3 LYSO scintillator, the coincidence timing resolution (CTR) changed by less than 3% within the range of 4 to 484 implemented TDCs for evaluated system conditions. On the other hand, an LYSO-based photonic crystal with 2.5% prompt emission rate needs a detector with at least 36 TDCs to reach within 3% CTR of an equivalent array with one TDC per SPAD. This gives significant insights on how this change of crystal material will affect system real time requirements for future detector design.

***Index Terms*—Scintillation photon detection, prompt photons, time of flight, SiPM, digital SiPM, Time to Digital converter, Coincidence Timing Resolution, Positron Emission Tomography, detector design**

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I. Introduction

TIME-OF-FLIGHT measurement in positron emission tomography (PET) is a well know technique to increase the contrast to noise ratio, but requires very fast timing performances. While clinical systems can benefit from detectors providing 500 ps FWHM coincidence timing resolution (CTR) or less, pre-clinical systems must reach well below 100 ps FWHM to achieve similar benefits in the image because of the much smaller studied volumes. Furthermore, if detectors were to reach the 10 ps FWHM threshold, direct image reconstruction would be possible with 1.5 mm FWHM spatial resolution on the line of response [1], bypassing complex iterative image reconstruction algorithms.

SiPM design has received much attention over the past 15 years, but only in the last 5 years have appeared fully digital arrays dedicated to PET. Unlike SiPM, digital SPAD arrays can timestamp several [2] or every SPAD cell that triggers during an scintillation event. Multiple photon timestamping in turn enables signal processing based on photon statistics [3], [4], [5]. Digital SPAD arrays may also disable abnormally noisy cells and usually include active hold-off circuits to reduce afterpulsing [6], [2]. The readout signal is sent off-chip directly in digital form, removing the circuit board from the noise sensitive timing pathway.

Although a configuration with one TDC per SPAD cell will guarantee the best possible sampling, it involves heavy system design requirements and does not necessarily provide the best resource usage to performance ratio. Furthermore, large arrays of TDC occupy significant real-estate, leaving little room for on-die real-time processing. Offloading the data to FPGA does circumvent the problem, but at the price of using several transmission lanes, raising the devices power consumption and connection density. This paper proposes a simulation-based analysis flow to determine the embedded requirements of a multi-TDC digital SPAD array optimized for a given scintillator material. Although electronic jitter should be minimized de facto, the amount of TDCs to be implemented is also an important parameter at the system design level. First, the flow is applied to a standard LYSO. Then the flow is applied to a LYSO-like crystal that includes a small fraction of prompt photons [7]. The goal is to determine how many TDCs are really needed to reach the 10 ps FWHM CTR goal

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for PET with reasonable real-time requirements, what would be an acceptable overall electronic jitter, what are the required TDC precision and jitter (or resolution), and what tradeoffs between these factors are available.

II. Trade-offs

In any SPAD based PET detector, the CTR is strongly affected by the optical fill factor under the scintillator crystal. Digital SPAD array designers must therefore balance it against embedded electronics size and performance, thus the usefulness of this simulation tool. On the other hand, by using vertical electronic integration, this constraint is greatly relaxed, and the optical and electronic design efforts can be cleanly separated. Electronic design can then focus on tradeoffs between embedded features, system architecture, timing precision and jitter considerations. Good timing being a key feature, electronic jitter, the TDC count, their precision and jitter all become central issues in these designs.

III. Materials and Methods

The scintillators were simulated using the Geant4 toolkit. It provides the detailed simulation for light generation, light dispersion, reflector material impact and light absorption in the detector material. The prompt photons in the crystal are emulated through a second scintillation component with very fast rise and decay time (0.1 and 5 ps respectively) and a 2.5% relative light yield (or about 500 generated prompt photons). The SPAD array is simulated with a physical model [8], which includes the avalanche process, quenching circuit jitter and the dynamic non-linearity incurred by quenching dead time. The layout has 22 x 22 SPAD cells with a 50 um step and an effective PDE of 18%. Dark counts were not considered in this study. A separate TDC model with variable precision and jitter completes the DAQ chain. The gamma detection time mark calculation is then applied using a first photon estimator (FPE) [6], [9] and a Maximum Likelihood Estimator (MLE) [3], [4], [5].

IV. Results

A. Standard LYSO

Figures 1 shows the CTR obtained with a fixed SPAD cell jitter (J_{Cell}) of 30 ps FWHM, fixed 1 ps precision and variable TDC jitter. The lower bound is similar to other simulation methodologies [4]. At medium and high total jitter levels, MLE increasingly improves the CTR over the one obtained by the very simple but efficient first photon estimator. However, at low jitter, MLE provides little improvement over FPE. Furthermore, figure 2 shows that the number of TDCs in the system doesn't significantly change the obtained MLE CTR for different TDC precisions. Detectors for standard LYSO scintillators should not create needless real time requirements by embedding excessive amounts of TDCs. Rather, the silicon real-estate should be used to optimize overall jitter performance or embed extra features such as smarter quenching circuits with better timing performance. At very low jitter, using multiple TDCs has little contribution to CTR improvement and the first photon estimator becomes very cost-effective and requires virtually no real time processing requirements.

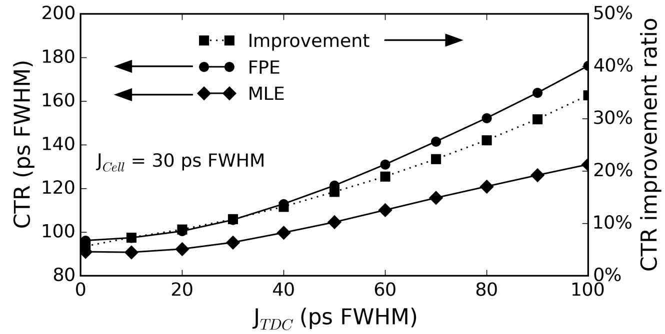

Fig. 1. CTR for both the FPE and the MLE estimators for a LYSO scintillator with fixed cell jitter (J_{Cell}) and different TDC jitter (J_{TDC}) with a 1 ps precision TDC (1 ps LSB).

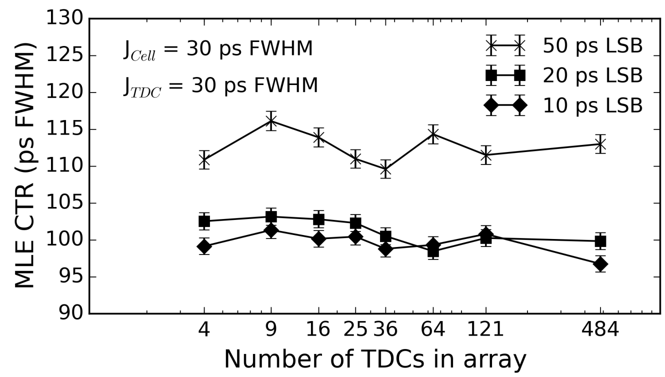

Fig. 2. MLE CTR for standard LYSO with different TDC instance counts in the SPAD array and different TDC precisions (LSB). Error bars represent a 95% confidence interval.

B. Photonic Crystal (LYSO with prompts)

Figure 3 shows the CTR obtained with 500 additional generated prompt photons, a SPAD cell jitter of 15 ps FWHM, fixed 1 ps precision TDC with variable jitter. CTR almost reaches the 10 ps FWHM CTR goal when the TDC has less than 5 ps FWHM of jitter. Figure 4 indicates that the number of instantiated TDCs does affect the result in this case. This is because the arrival rate of prompt photons is much higher than LYSO scintillation, and MLE can contribute more strongly to reduce uncertainties. The results also suggest that one TDC per SPAD is not necessary, and that a small sharing ratio scheme will not deteriorate CTR overmuch.

V. Conclusion

Digital SPAD arrays with one TDC per SPAD cell will certainly be useful for detector material characterization. However, these devices will generate very large amounts of data that will likely need to be processed off-chip. PET systems would benefit both in terms of power and real-time processing requirements if TDC sharing schemes are used instead.

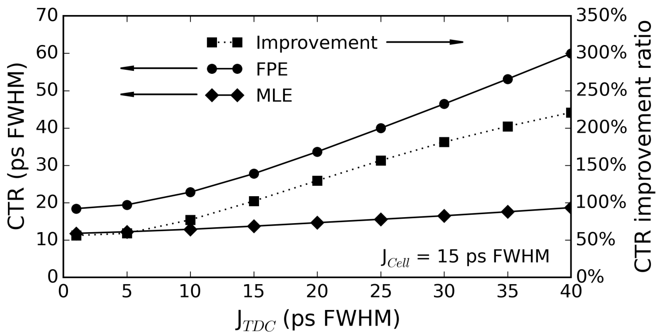

Fig. 3. CTR for both the FPE and the MLE estimators for a LYSO-based photonic crystal with fixed cell jitter (J_{Cell}) and varying TDC jitter (J_{TDC}) with a 1 ps precision TDC (1 ps LSB).

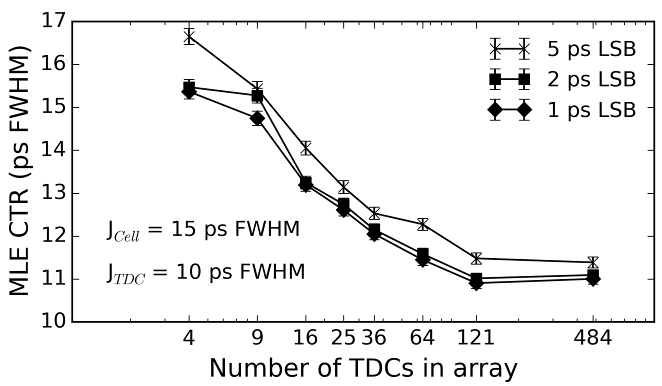

Fig. 4. MLE CTR for a LYSO-like photonic crystal with different TDC instance counts in the SPAD array and different TDC precisions (LSB). Error bars represent a 95% confidence interval.

Furthermore, the freed real-estate can be used to implement better TDCs, which will be required to reach the 10 ps FWHM system CTR goal.

New SPAD devices can thus be designed with either low-cost or maximum performance and tailored for the detecting material properties.

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